Technical Manual BI-1508
ECN Voltage Monitoring System

Version 2.0 March 2001

Documentation History

Date	Version	PCB Revision	Update Level	Change/Description
2000/02/04	0.0	0.0	-	Not released
2000/04/14	1.0	1.0	A	First issue
2000/05/08	1.1	1.0	A	Editorial changes
2001/03/02	2.0	2.0	-	Replaced SRAM/Flash/Glue by PSD

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Chapter 1

General Information

1.1 Introduction

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the BI-1508. The manual also includes basic information needed by software engineers to design and implement software for the module.

1.2 Voltage Monitoring System Description

The purpose of the Voltage Monitoring System (VMS) is to measure the individual voltage of a cell, or a group of cells of a fuel cell stack. A single VMS-module can monitor 40 voltages within a maximum input voltage range of 150 Volt DC. VMS-modules can be placed in series; a total voltage range of 500 Volt DC (optionally >500 Volt DC) is thereby covered. A group of cells may consist of maximum 4 cells (depends on gain setting ADC of VMS-board).

Each VMS-module contains a microprocessor, which measures and checks the 40 voltages with a sample rate of 2 samples per second. In case one of the voltages is out of a safe range a relay-contact is opened which can be used to control or shut-down the fuel processor, or disconnect the fuel cell stack from the load i.e. the power consumer.

The system contains a CAN-interface via which a master-control unit is able to communicate which each individual VMS-board. The master is able read the individual cell voltages in real time, and is also able to set the alarm levels. The functionality of the VMS-module can be adapted by reprogramming the on-board microprocessor.

1.3 Specifications CAN VMS system

- VMS is a modular concept: VMS modules can be placed in series as long as the total DC voltage of a stack is below 500 Volt DC, 1 VMS module contains 40 analog input channels
- Common mode voltage range per VMS module +150 Volt DC
- Common mode voltage range total VMS system is 500 Volt DC
- Sample rate for all cells: 2 samples per second
- Input channel voltage range 0 to 5.0 Volt
- Cell voltage resolution: ca 0.005 Volt
- Absolute accuracy: < 0.015 Volt (measured at a common mode voltage of 40 Volt), if reference (signal ground) connected in the middle of the stack, < 0.010 Volt can be guaranteed
- Galvanic isolated CAN transceiver (>500 Volt DC)
- Galvanic isolated RS232 serial port (>500 Volt DC)
- Power supply: 24 Volt DC (isolation between input/output > 1500 Volt)

- 2 optocoupler output contacts: programmable for “warning” alarm and “fatal” alarm
- Cell voltage connector is a 44 pole high density 'D' connector
- The boards are programmable and can be adapted to fulfil different functionality
- Operational temperature range: 0- 50 degrees Celsius (-20 to +70 on request)
- Dimensions: Eurocard format each module (100 * 160 * 20 mm).

1.4 Features

The features of the BI-1508 module include:

Local Processor

- SAF-C515C 8-bit micro-controller, 16 bit address, 8 bit data, 10 MHz
- Uses 80C51 instruction set

CAN Compatible

- One CAN interface channel using C515C on-chip CAN controller
- 1 Mbit/sec CAN-controller
- ISO/DIS 11898 high speed physical interface with optical isolation

Local Memory

- 256 bytes Data Memory, internal
- 2 kByte XData Memory, internal
- 32 kByte Flash Boot Memory, 8 bit wide, external
- 256 kByte Flash Main Memory, 8 bit wide, external
- 32 kByte SRAM, 8 bit wide, external
- 512 byte Serial EEPROM, external

I/O Ports

- 5 x 8 analog inputs, input range 0 - 5 Vdc, 12-bit resolution
- 2 x high current output switches with optical isolation
- RS-232 asynchronous serial port with optical isolation
- Module ID inputs for geographical addressing of the module

Miscellaneous Functions

- Power monitor and watchdog
- Supply voltage monitoring on +5Vdc, +15Vdc and -15Vdc

1.5 General Description

The BI-1508 is designed to measure 40 voltage inputs between 0 and 5 Vdc each and to transmit the acquired measurements in CAN messages to the CAN network.

The 40 input voltage inputs are cascaded giving a overall input range of 200 Vdc.

$$40 \times 5 \text{ Vdc} = 200 \text{ Vdc} \quad \textbf{(EQ 1)}$$

Each input voltage is connected to a a precision unity-gain difference amplifier with very high common-mode input voltage range. Each amplifier can accurately measure small differential voltage inputs in the presence of common-mode signals up to ±200V. The amplifier inputs are protected from momentary common-mode or differential overloads up to ±500V. Each input includes a 20 Hz filter low pass filter.

The BI-1508 provides five analog to digital converters with eight analog inputs each with an input range of 0 to 5 Vdc for each input. The converters deliver 12-bit samples at a maximum sampling rate of 16,800 samples per second. The actual sample rate is determined by software through the C515C micro-controller.

The module contains a CAN network interface connection, using the on-chip CAN controller and an accompanying physical network interface. The maximum bit rate is 1 Mbit, the actual bit rate is determined by software. The physical interface is conform the ISO/DIS 11898 standard using the PCA82C251 CAN transceiver. To provide additional protection, the interface is optically isolated using on-board optocouplers and DC/DC converter.

1.6 Manual Updates

Table 1-1 Manual Updates

Revision	Changes	Additions	Deletions
1.0			
2.0			

1.7 Ordering Information

The next table gives an overview of the different options that are available for the BI-1508.

Table 1-2 Ordering Information

Function	Options
Microprocessor Option	SAF-C515C-L
Code Memory	256 + 32 kByte External Flash EPROM
Data Memory	2 kByte Internal SRAM + 32 kByte External SRAM

1.8 Related Documents

The following documentation can be referred to for detailed information about related items not described in this manual.

Table 1-3 List of Documents

Document Title	Published by	PDF File
SAF-C515C 8-bit micro-controller with on-chip CAN Data Sheet	Infineon	c515c.pdf
LH1522 High Voltage Solid State Relays	Infineon	lh1522.pdf
PCA82C251 24V CAN Transceiver Data Sheet	Philips Semiconductors	pca82c251.pdf
TL7702 Supply Voltage Supervisor Data Sheet	Texas Instruments	tl7702b.pdf
PSD854F2 Flash In-System-Programmable Microcontroller Peripherals	STMicroelectronics	psd854f2.pdf
AT25040 SPI Serial CMOS EEPROM Data Sheet	Atmel	at25040.pdf
LTC1594/LTC1598 4- and 8-Channel, Micropower Sampling 12-Bit Serial I/O A/D Converters	Linear Technology	ltc1598.pdf
LT1634 Micropower Precision Shunt Voltage Reference	Linear Technology	lt1634a.pdf
AD629 High Common-Mode Voltage Difference Amplifier	Analog Devices	ad629.pdf
HCPL-7710 40 ns Propagation Delay, CMOS Optocoupler	Hewlett-Packard	hcpl7710.pdf

Chapter 2

Specifications

2.1 Introduction

The BI-1508 is equipped with the C515C micro-controller from Infineon. The optical isolated physical interfaces is based on the PCA82C251 CAN transceiver.

2.2 Components Used

The following section gives an overview of the main parts that are used.

2.2.1 C515C

The SAF-C515C is a single-chip 8-bit high-performance micro-controller with on-chip CAN-controller, derived from the 80C51 micro-controller family. It uses the powerful 80C51 instruction set.

The C515C key features are:

- On-chip program memory (with optional memory protection)
  C515C-L: 0k byte on-chip ROM
  C515C-8R: 64k byte on-chip ROM
  C515C-8E: 64k byte on-chip OTP
  alternatively up to 64k byte external program memory
- 256 byte on-chip RAM
- 2K byte on-chip XRAM
- Up to 64K byte external data memory
- Super set of the 8051 architecture with 8 data pointers
- Up to 10 MHz external operating frequency without clock prescaler
  (1 us instruction cycle time at 6 MHz external clock)
- On-chip emulation support logic (Enhanced Hooks Technology^{TM})
- Current optimized oscillator circuit
- Eight ports: 48 + 1 digital I/O lines, 8 analog inputs
  Quasi-bidirectional port structure (8051 compatible)
  Port 5 selectable for bidirectional port structure (CMOS voltage levels)
- Three 16-bit timer/counters
  Timer 2 can be used for compare/capture functions
- 10-bit A/D converter with multiplexed inputs and Built-in self calibration
- Full duplex serial interface with programmable baud rate generator (USART)

- SSC synchronous serial interface (SPI compatible)
  - Master and slave capable
  - Programmable clock polarity / clock-edge to data phase relation
  - LSB/MSB first selectable
  - 2.5 MHz transfer rate at 10 MHz operating frequency
- Full-CAN Module
  - 256 register/data bytes are located in external data memory area
  - maximum 1 MBaud at 10 MHz operating frequency
- Seventeen interrupt vectors, at four priority levels selectable
- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake-up capability through INT0 or RXDC pin
  - Hardware power-down mode
- CPU running condition output pin
- ALE can be switched off

2.2.2 On-chip CAN Controller

CAN is the definition of a high performance communication protocol for serial data communication. The C515C on-chip CAN-controller is a full implementation of the CAN 2.0B protocol. With the C515 powerful local networks can be built, both for automotive and general industrial environments. This results in a much reduced wiring harness and enhanced diagnostic and supervisory capabilities. It provides a sophisticated object layer to relieve the CPU of as much overhead as possible when controlling many different message objects (up to 15).

The CAN features are:

- Multi-master architecture
- Bus access priority determined by the message identifier
- Standard CAN protocol (11-bit identifiers)
- Extended CAN protocol (29-bit identifiers).
- Guaranteed latency time for high priority messages
- Powerful error handling capability
- Data length from 0 up to 8 bytes
- Multicast and broadcast message facility
- Non destructive bit-wise arbitration
- Non-return-to-zero (NRZ) coding/decoding with bit-stuffing
- Programmable transfer rate (up to 1 Mbit/s)
- Suitable for use in a wide range of networks including the SAE's network classes A, B and C

The PCA82C251 is the standard interface between the CAN protocol controller and the physical bus. It is intended for high speed applications up to 1 MBaud and is fully compatible with the ISO/DIS 11898 standard.

2.2.3 Memory Devices

External Flash and SRAM memory is available through the PSD854F2 Programmable Microcontroller (MCU) Peripheral. This part provides 2 Mbit of Flash memory, a second Flash Boot memory and 256 Kbit SRAM.

- Internal 2 Mbit Flash memory.

  This is the main Flash memory. It is divided into eight equal-sized blocks that can be accessed with user-specified addresses.
- Internal secondary 256 Kbit Flash boot memory.

  It is divided into four equal-sized blocks that can be accessed with user-specified addresses. This secondary memory brings the ability to execute code and update the main Flash concurrently.
- Internal 256 Kbit SRAM.

  The SRAM's contents can be protected from a power failure by connecting an external battery.
- CPLD with 16 Output Micro Cells (OMCs) and 24 Input Micro Cells (IMCs).

  The CPLD may be used to efficiently implement a variety of logic functions for internal and external control. Examples include state machines, loadable shift registers, and loadable counters.
- Decode PLD (DPLD) that decodes address for selection of internal memory blocks.
- 27 individually configurable I/O port pins that can be used for the following functions:
  MCU I/Os
  PLD I/Os
  Latched MCU address output
  Special function I/Os.
  16 of the I/O ports may be configured as open-drain outputs.
- Stand-by current as low as 50 µA for 5 V devices.
- Built-in JTAG compliant serial port allows full-chip In-System Programmability (ISP).

  With it, you can program a blank device or reprogram a device in the factory or the field.
- Internal page register.

  This can be used to expand the microcontroller address space by a factor of 256.
- Internal programmable Power Management Unit (PMU).

  This supports a low power mode called Power Down Mode. The PMU can automatically detect a lack of microcontroller activity and put the PSD8XXF into Power Down Mode.
- Erase/Write cycles:
  Flash memory – 100,000 minimum
  PLD – 1,000 minimum
  Data Retention: 15 year minimum (for Main Flash, Boot, PLD and Configuration bits)

The non-volatile memory consists of a 512 bytes serial E^2PROM AT25040 which features a Serial Peripheral Interface (SPI) compatible interface and a Write Disable instruction for software data protection.

2.2.4 Analog to Digital Converter

The LTC1598 is a micropower, 12-bit sampling A/D converter that features an 8-channel multiplexer. It typically draws only 320mA of supply current when converting and automatically powers down to a typical supply current of 1nA between conversions. It operates on a 5V supply. The 12-bit, switched-capacitor, successive approximation ADCs include a sample-and-hold. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and micro-controllers over three or four wires.

This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

Features of the LTC1598 are:

- 12-Bit Resolution
- Auto Shutdown to 1nA
- Low Supply Current: 320mA Typical
- Guaranteed ±3/4LSB Maximum DNL
- Single Supply 5V Operation
- Multiplexer: 8-Channel MUX (LTC1598)
- Separate MUX Output and ADC Input Pins
- MUX and ADC May Be Controlled Separately
- Sampling Rate: 16.8ksps
- I/O Compatible with QSPI, SPI and MICROWIRE

2.2.5 Unity-gain Difference Amplifier

The AD629 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision operational amplifier and integrated thin-film resistor network. It can accurately measure small differential voltage inputs in the presence of common-mode signals up to ±270V. The AD629 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the AD629 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The AD629's 0.001% non-linearity and 500kHz bandwidth are superior to those of conventional isolation amplifiers.

The features of the AD629 are:

- Common-mode input range ±270V (V_S = ±15V)
- Protected inputs, ±500V Common-Mode, ±500V Differential
- Unity gain 0.02% gain error maximum
- Non-linearity 0.001% maximum
- CMRR: 86dB minimum

2.3 Output Contacts

Two high current switches, Warning and Fatal are implemented with the Siemens LH1522 Solid State Relays (SSR). They are miniature, optically-coupled relays with high-voltage MOSFET outputs. The relays are capable of switching AC or DC loads from as little as nano-volts to hundreds of volts. Likewise, the relays can switch currents in the range of nano-amps to hundreds of milli-amps. The MOSFET switches are ideal for small signal switching and are primarily suited for dc or audio frequency applications.

2.4 Input/Output Options

Analog Interface Options

- Five times eight analog inputs
- Input range 0 - 5 Vdc

CAN Options

- One CAN channel
- ISO/DIS 11898 compatible isolated physical interface

Serial Interface Options

- Asynchronous RS-232 with isolated physical interface

Miscellaneous

- Front panel LED for Warning, Fatal and Processor Status
- Power supply connector accepts 24 Vdc @ 5 W Maximum

2.5 Specifications

The BI-1508 specifications are given in the next table.

Table 2-1 Specifications

Characteristics	Specifications
Power requirements	24 Vdc @ 5 W (maximum)
Operating temperature	0 to +70 degrees C ambient air temperature
	-20 to +70 degrees C ambient air temperature
Storage temperature	-25 to +85 degrees C
Relative humidity	5% to 90% (non-condensing)
Dimensions	
Width	100 mm
Depth	160 mm
Thickness	20 mm

Chapter 3

Installation Procedures

3.1 Introduction

This chapter provides the preparation and installation instructions for the BI-1508.

3.2 Installation

The module is shipped in an antistatic container to protect the module against static electricity. When the module is unpacked, avoid touching areas of integrated circuitry to prevent static discharge from damaging the circuits.

Jumpers are used to select hardware specific options. The jumper block positioning and default jumper settings are illustrated in Appendix C.

3.3 Option Settings

The next table gives a summary of the available options, their default settings and their functions.

Table 3-1 Default Option Settings

Description	Selection	Default Setting	Status	Section
Slope Control	R24	Inserted	Normal mode	3.3.1
Watch Dog Enable	R25	Inserted	Watchdog is disabled	3.3.2
Push Button Reset	JB4	Empty	Reset is not active	3.3.3
Debug Select	JB2	2 - 3 connected	Debugger Disabled	3.3.4
Option Select	JB1	Empty	Software dependent	3.3.5

3.3.1 Slope Control

When using the standard CAN physical interface, the slope control mode allows the use of an unshielded twisted pair as bus lines. To reduce RFI, the rise and fall slope should be limited. The rise and fall slope is programmed using a 47 kOhm resistor when R24 is removed. When R24 is placed, no slope control is active and the interface can be operated using its highest speeds.

Table 3-2 Slope Control Selection

Selection	Slope Control	Normal Mode (default)
R24	Removed	Inserted

3.3.2 Watch Dog Enable

The watchdog timer can be set to reset the microprocessor when the watchdog is not kicked prior to the 1.0 second time-out. The watchdog can be enabled by removing R25.

Table 3-3 Watch Dog Enable

Jumper	Watchdog is enabled	Watchdog is disabled (default)
R25	Removed	Inserted

3.3.3 Push Button Reset

The push-button jumper can be connected to an external switch to reset the microprocessor. The processor will be reset when the switch is closed. The push-button input is debounced and an active reset pulse of 250 ms minimum is guaranteed.

Table 3-4 Push Button Reset

Jumper	Position	Description
JB4	Empty	Reset the microprocessor on the BI-1508

3.3.4 Debug Select

This jumper can be used to select the debug option.

Table 3-5 Debug Select

Jumper	Position	Description
JB2	1-2	Debugger Enabled
	2-3	Debugger Disabled

3.3.5 Option Select

This jumper can be used to select an option from the software. The meaning of this jumper is software defined.

Table 3-6 Option Select

Jumper	Position	Description
JB1	1-2	
	2-3	

3.4 Analog Input Connection

The next rules apply for the analog inputs VI_x where VI_x is in the range VI_{00} to VI_{40}:

1. The voltage on VI_{x+1} must never be lower than the voltage on VI_x.

This rule prevents the inputs to the AD converters to go negative. Note that any unused VIx+1 should be connected to VIx to meet this rule.

2. The voltage on VI_{x+1} must never be higher than the voltage on VI_x plus 5Vdc.

   This rule prevents the inputs to the AD converters to go above the supply voltage.

3. The voltage on VI_x must never be 200Vdc higher or lower than GND.

   Grounding should be done in a way that the common mode voltage is minimised.

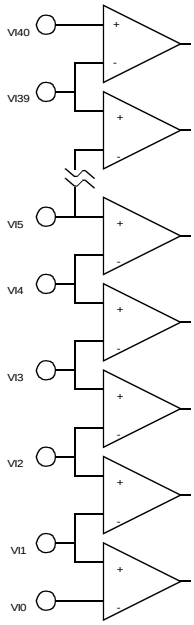

Figure 3-1 Input Connections

3.5 CAN Channel Connection

The CAN physical interface uses the power from the DC/DC converter. For signal pin assignment, signal direction and connector type, see Table E-3, “DIN-96 Pinning” on page E-2.

3.6 RS-232 Connection

The BI-1508 provides the send and transmit data signals. For signal pin assignment, signal direction and connector type, see Table E-2, “RS-232 Connector” on page E-1.

3.7 Power Supply Connection

The BI-1508 requires a single, 24 Vdc @ 5 W maximum, power supply for operation. For signal pin assignment, signal direction and connector type, see Table E-3, “DIN-96 Pinning” on page E-2.

3.8 FATAL and WARNING Switch Connection

The FATAL and WARNING switches are open when an error is to be reported. This allows the system to detect faulty wiring and missing boards. The FATAL and WARNING connections have no polarity.

3.9 Module ID Connection

The Module ID can be defined through the switched SW1 and SW2 or by the Module ID pins on the DIN-96 connector. When the DIN-96 connector pins are used for Module ID then the SW1 and SW2 switches must be set to 0xFF.

3.10 In System Programming Connection

For signal pin assignment, signal direction and connector type, see Table E-4, “In System Programming” on page E-2.

Chapter 4

Functional Description

4.1 Introduction

This chapter gives an overview of the BI-1508 module and a detailed description of the functional sections. The block diagram of the module is given in Appendix A and the schematic diagrams are given in Appendix B.

4.2 C515C Microcontroller

The Infineon C515C is the main processor on the BI-1508.

4.3 Clock Generation

One clock source is used for all devices in the BI-1508 design.

4.4 Reset Circuits

The BI-1508 supports three reset sources.

1. The TL7702 Supply Voltage Supervisor monitors the power supply and generates an automatic reset at power on or after a voltage drop.
2. A manual reset can be done through the TL7702.
3. A Watchdog Timer (WDT) is provided by the microcontroller. When a WDT timer overflow occurs, the microcontroller is reset and a reset-output-pulse is generated at pin RST.

4.4.1 Power Supply Monitor Reset

The TL7702 Supply Voltage Supervisor monitors the power supply value and will assert reset when the supply drops below 4.50 Vdc. When the power supply falls below 4.50 volts, the processor is stopped by asserting the reset input. On power up, reset is kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

4.4.2 Manual Reset

A jumper header is provided to reset the processor. This header can be connected to a separate external reset button when needed.

4.4.3 Hardware Watchdog Circuit Reset

The watchdog timer of the C515C must be stimulated or it will reset the processor. The watchdog must be kicked at regular intervals. When the hardware watchdog must be disabled, input EW can be connected to a high level using the jumper.

4.5 Serial Peripheral Interface

Serial Peripheral Interface (SPI) is a full-duplex, synchronous, character-orientated channel that supports a four-wire interface (receive, transmit, clock and slave select).

SCLK is the clock output, SRI is the receiver input, STO is the transmitter output. SLS is not used as the SPI select to the microcontroller and can be used as a general purpose I/O. The SLS input is disabled in the master SPI mode.

Table 4-1 Devices on the SPI

Device	Device Name
Serial EEPROM	AT25040

4.6 Testability

The BI-1508 contains mostly Surface Mounted Devices (SMD). Therefore Boundary Scan Test (BST) methodology has been implemented to make production possible. This methodology is used to program the In-System Programmable (ISP) logic.

4.6.1 ISP Connector

The ISP connector is connected to the ISP interface signals of the PSD854F2.

4.7 Interrupts

The BI-1508 provides several internal and external interrupt sources. The internal interrupt sources are fully described in the C515C users manual. The external interrupt sources are given in the following table.

Table 4-2 External Interrupt Sources

Port	Name	Usage
Port1.5	T2EX	Not used as interrupt source
Port3.2	$\overline{\text{INT0}}$	Not used as interrupt source
Port3.3	$\overline{\text{INT1}}$	Not used as interrupt source
Port1.4	$\overline{\text{INT2}}$	Not used as interrupt source
Port1.0	$\overline{\text{INT3}}$	Not used as interrupt source

Table 4-2 External Interrupt Sources

Port	Name	Usage
Port1.1	INT4	Not used as interrupt source
Port1.2	INT5	Not used as interrupt source
Port1.3	INT6	Not used as interrupt source
Port7.0	$\overline{\text{INT7}}$	Not used as interrupt source
Port4.5	$\overline{\text{INT8}}$	Not used as interrupt source

Chapter 5

Programming Considerations

5.1 Introduction

This section contains all necessary information for programmers to take full advantage of the features of the BI-1508 module. The descriptions will include implementation dependent information that cannot be found in the respective data sheets.

This chapter should be used in conjunction with the references given in “Related Documents” on page 1-4. System programmers are expected to be fully conversant with all the material and have the relevant experience before writing their own system software.

Appendix F shows the Memory map and the I/O map of the BI-1508 module.

5.2 Register Settings for the C515C

The microcontroller internal registers must be programmed after hardware reset as described in the following paragraphs. The addresses and programming values are in hexadecimal base.

After reset, the port latches are set to 0xFF. This leaves port 0 floating, since it is an open drain port when not used as data/address bus. All other I/O port lines (ports 1 to 5 and 7) output a one (1). Port 6 is an input-only port. It has no internal latch and therefore the contents of the special function registers P6 depend on the levels applied to port 6.

Please refer to the C515C User’s Manual for more information.

5.2.1 Port 0 Assignments

Low level output voltage 0.45 V @ 3.2 mA.
High level output voltage 2.4 V @ -800 uA.

Table 5-1 Port 0 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port0.0	AD0	In/Out	AD0	10 kOhm
Port0.1	AD1	In/Out	AD1	10 kOhm
Port0.2	AD2	In/Out	AD2	10 kOhm
Port0.3	AD3	In/Out	AD3	10 kOhm
Port0.4	AD4	In/Out	AD4	10 kOhm
Port0.5	AD5	In/Out	AD5	10 kOhm

Table 5-1 Port 0 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port0.6	AD6	In/Out	AD6	10 kOhm
Port0.7	AD7	In/Out	AD7	10 kOhm

5.2.2 Port 1 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-2 Port 1 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port1.0	$\overline{\text{INT3}}$/CC0	Out	ADC Clock 0	No
Port1.1	INT4/CC1	Out	ADC Clock 1	No
Port1.2	INT5/CC2	Out	ADC Clock 2	No
Port1.3	INT6/CC3	Out	ADC Clock 3	No
Port1.4	$\overline{\text{INT2}}$	Out	ADC Clock 4	No
Port1.5	T2EX	-	-	No
Port1.6	CLKOUT	-	-	No
Port1.7	T2	-	-	No

5.2.3 Port 2 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-3 Port 2 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port2.0	A8	Out	A8	No
Port2.1	A9	Out	A9	No
Port2.2	A10	Out	A10	No
Port2.3	A11	Out	A11	No
Port2.4	A12	Out	A12	No
Port2.5	A13	Out	A13	No
Port2.6	A14	Out	A14	No
Port2.7	A15	Out	A15	No

5.2.4 Port 3 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-4 Port 3 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port3.0	RXD/DATA	In	RXD RS-232	No
Port3.1	TXD/CLOCK	Out	TXD RS-232	No
Port3.2	$\overline{\text{INT0}}$	-	-	No
Port3.3	$\overline{\text{INT1}}$	Out	FATAL	No
Port3.4	T0	Out	$\overline{\text{HEALTHY}}$	No
Port3.5	T1	Out	WARNING	No
Port3.6	$\overline{\text{WR}}$	Out	$\overline{\text{WR}}$	No
Port3.7	$\overline{\text{RD}}$	Out	$\overline{\text{RD}}$	No

5.2.5 Port 4 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-5 Port 4 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port4.0	$\overline{\text{ADST}}$	Out	CS EEPROM	No
Port4.1	SCLK	Out	CLK EEPROM	No
Port4.2	SRI	In	DATA EEPROM	10 kOhm
Port4.3	STO	Out	DATA EEPROM	No
Port4.4	$\overline{\text{SLS}}$	Out	ADC Data In (0 to 4)	No
Port4.5	$\overline{\text{INT8}}$	-	-	No
Port4.6	TXDC	Out	CAN Data	10 kOhm
Port4.7	RXDC	In	CAN Data	No

5.2.6 Port 5 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-6 Port 5 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port5.0	I/O	Out	ADC $\overline{\text{CS}}$ 0	No
Port5.1	I/O	Out	ADC $\overline{\text{CS}}$ 1	No
Port5.2	I/O	Out	ADC $\overline{\text{CS}}$ 2	No
Port5.3	I/O	Out	ADC $\overline{\text{CS}}$ 3	No
Port5.4	I/O	Out	ADC $\overline{\text{CS}}$ 4	No

Table 5-6 Port 5 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port5.5	I/O	-	-	No
Port5.6	I/O	-	-	No
Port5.7	I/O	-	-	No

5.2.7 Port 6 Assignments

This port is an inputs only port.

Table 5-7 Port 6 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port6.0	ADC0	In	ADC Data Out 0	10 kOhm
Port6.1	ADC1	In	ADC Data Out 1	10 kOhm
Port6.2	ADC2	In	ADC Data Out 2	10 kOhm
Port6.3	ADC3	In	ADC Data Out 3	10 kOhm
Port6.4	ADC4	In	ADC Data Out 4	10 kOhm
Port6.5	ADC5	In	Monitor for +5 Vdc	Resistor Network
Port6.6	ADC6	In	Monitor for +15 Vdc	Resistor Network
Port6.7	ADC7	In	Monitor for -15 Vdc	Resistor Network

5.2.8 Port 7 Assignments

Low level output voltage 0.45 V @ 1.6 mA.
High level output voltage 2.4 V @ -80 uA.

Table 5-8 Port 7 Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
Port7.0	$\overline{\text{INT7}}$	-	-	No

5.3 Register Settings for the PSD854F2

5.3.1 Port A Assignments

Port A is used to read the Module ID signals. It is programmed in the MCU I/O mode and the Module ID can be read from the Port A Data In register in the CSIOP space.

Table 5-9 Port A Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
PortA.0	MCU I/O	In	Module ID 0	3.9 kOhm
PortA.1	MCU I/O	In	Module ID 1	3.9 kOhm
PortA.2	MCU I/O	In	Module ID 2	3.9 kOhm

Table 5-9 Port A Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
PortA.3	MCU I/O	In	Module ID 3	3.9 kOhm
PortA.4	MCU I/O	In	Module ID 4	3.9 kOhm
PortA.5	MCU I/O	In	Module ID 5	3.9 kOhm
PortA.6	MCU I/O	In	Module ID 6	3.9 kOhm
PortA.7	MCU I/O	In	Module ID 7	3.9 kOhm

5.3.2 Port B Assignments

Table 5-10 Port B Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
PortB.0	Combinatorial	Out	Healthy LED	No
PortB.1	Combinatorial	Out	Warning LED	No
PortB.2	Combinatorial	Out	Fatal LED	No
PortB.3	MCU I/O	In	Option Select from Jumper	No
PortB.4	Combinatorial	Out	Warning to Solid State Relay	No
PortB.5	Combinatorial	Out	Fatal to Solid State Relay	No
PortB.6	Logic Input	In	Warning from CPU	No
PortB.7	Logic Input	In	Fatal from CPU	No

5.3.3 Port C Assignments

Table 5-11 Port C Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
PortC.0	JTAG	In	TMS	3.9 kOhm
PortC.1	JTAG	In	TCK	1 kOhm (pull-down)
PortC.2	Logic Input	In	$\overline{\text{Healthy}}$ from CPU	No
PortC.3	JTAG	Out	TSTAT	3.9 kOhm
PortC.4	JTAG	Out	$\overline{\text{TERR}}$	3.9 kOhm
PortC.5	JTAG	In	TDI	3.9 kOhm
PortC.6	JTAG	Out	TDO	3.9 kOhm
PortC.7	MCU I/O	Out	Drives MOD signal	No

5.3.4 Port D Assignments

Table 5-12 Port D Usage

Pin name	Pin Function	Direction	Board Function	External Pull Up
PortD.0	Address Control	In	ALE from CPU	No
PortD.1	Common Clock	In	Clock 10 Mhz	No
PortD.2	Logic Input	In	Debug Select from Jumper	No

5.4 Peripherals

The following peripherals are available on the BI-1508:

Table 5-13 Peripherals

Name	Access	comment
Flash Memory	Memory Mapped	
SRAM	Memory Mapped	
CAN Port	Internal Device	
ADC Converters	Port Bits	
Module ID	PSD Registers	
Healthy, Warning and Fatal	Memory Mapped	
RS-232	Internal Device	
Serial EEPROM	Port Bits	

5.4.1 Flash Memory

No special considerations.

5.4.2 SRAM

The SRAM can be mapped to code space by setting the SRAM bit in the VM register. This feature is used during software debugging. Be aware that the SRAM will hide the Flash contents in this memory region.

5.4.3 CAN Port

No special considerations.

5.4.4 ADC Converters

The reference voltage for the ADC converters is 5.0 Volt. It is advised by the manufacturer of the ADC to keep the f_{clk} between 160 kHz and 320 kHz.

5.4.5 Module ID

The Module ID switches or the Module ID connections to the back plane connector can be read back through the Port A register in the PSD. Before the Module ID can be read, the Mod bit in Port C in the PSD must be set.

5.4.6 $\overline{\text{Healthy}}$, Warning and Fatal

The $\overline{\text{Healthy}}$, Warning and Fatal signals are driven by the following Port 3 outputs.

Table 5-14 Healthy, Warning and Fatal Usage

Pin Name	Function	After reset	LED Indicators	Solid State Outputs
Port3.3	Fatal Status	1	Fatal LED is ON	Fatal Switch is OPEN
Port3.4	Healthy Status	1	Healthy LED is OFF	
Port3.5	Warning Status	1	Warning LED is ON	Warning Switch is OPEN

The Healthy bit is connected to the Processor Status LED on the front. The Warning and Fatal bits are connected to the Warning and Fatal Status LEDs on the front and to the drivers for the Warning and Fatal output switches. The Healthy, Warning and Fatal bits are set to their initial values when the processor is reset through a power-up or watch-dog reset.

5.4.7 RS-232

The RS-232 port does not include any hardware handshake or modem signals.

5.4.8 Serial EEPROM

The AT25040 is a SPI compatible CMOS serial E^2PROM. It can contain 4k (512 x 8) bit of information and provides write protection in software.

5.5 LED Indicators

A variety of indicator LEDs are available on the BI-1508.

5.5.1 Processor Status LED

This is a green LED for the processor status. The LED is turned OFF when a power-up or watch-dog reset occurs. The processor can turn this LED ON and OFF through Port3.4.

5.5.2 Warning Status LED

This is a orange LED. This LED is turned ON when a power-up or watch-dog reset occurs. The processor can turn this LED ON and OFF through Port3.5. When this LED is on, the Warning switch will be open.

5.5.3 Fatal Status LED

This is a red LED. This LED is turned ON when a power-up or watch-dog reset occurs. The processor can turn this LED ON and OFF through Port3.3. When this LED is on, the Fatal switch will be open.

Appendix A Block Diagram

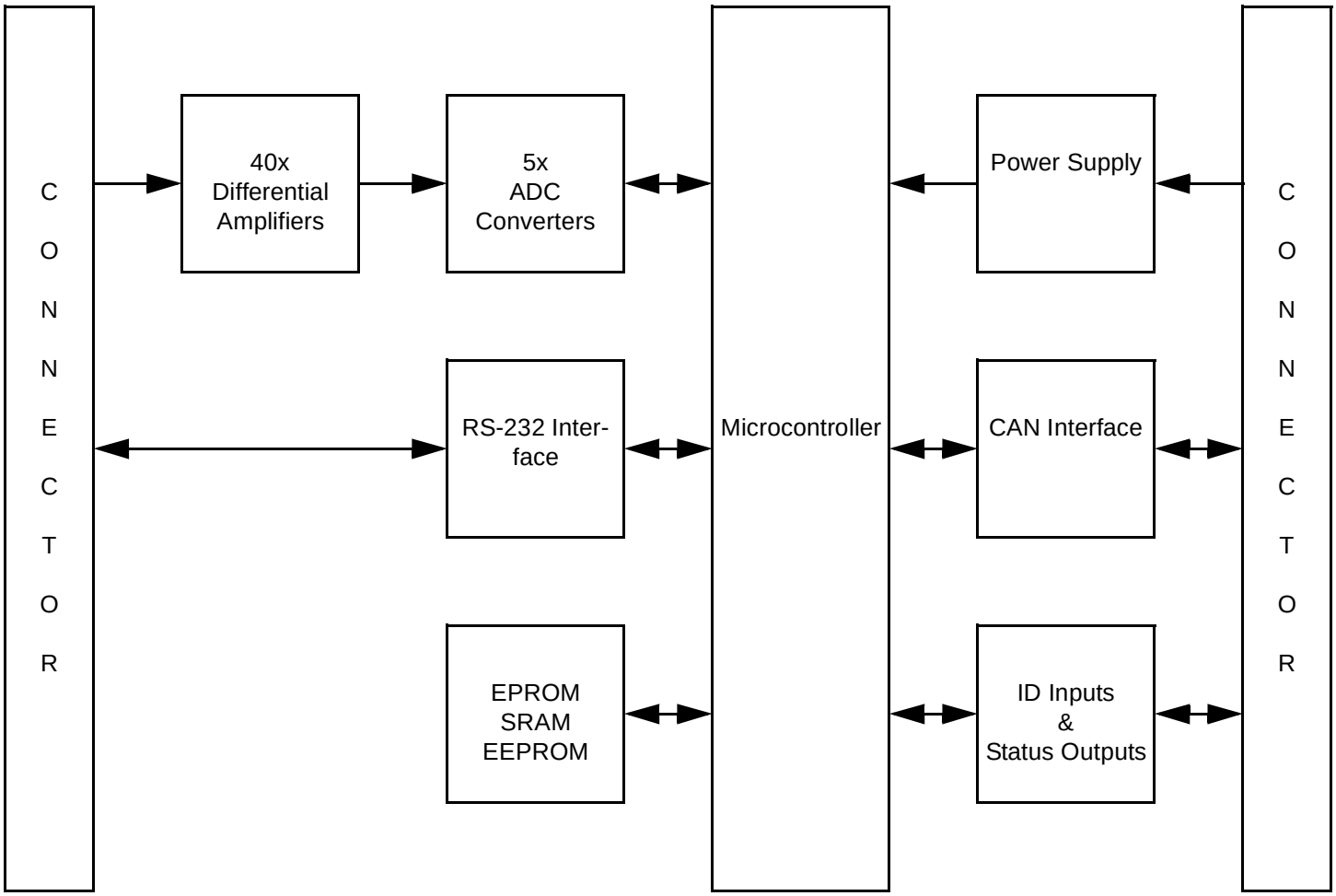

Figure A-1 Block Diagram

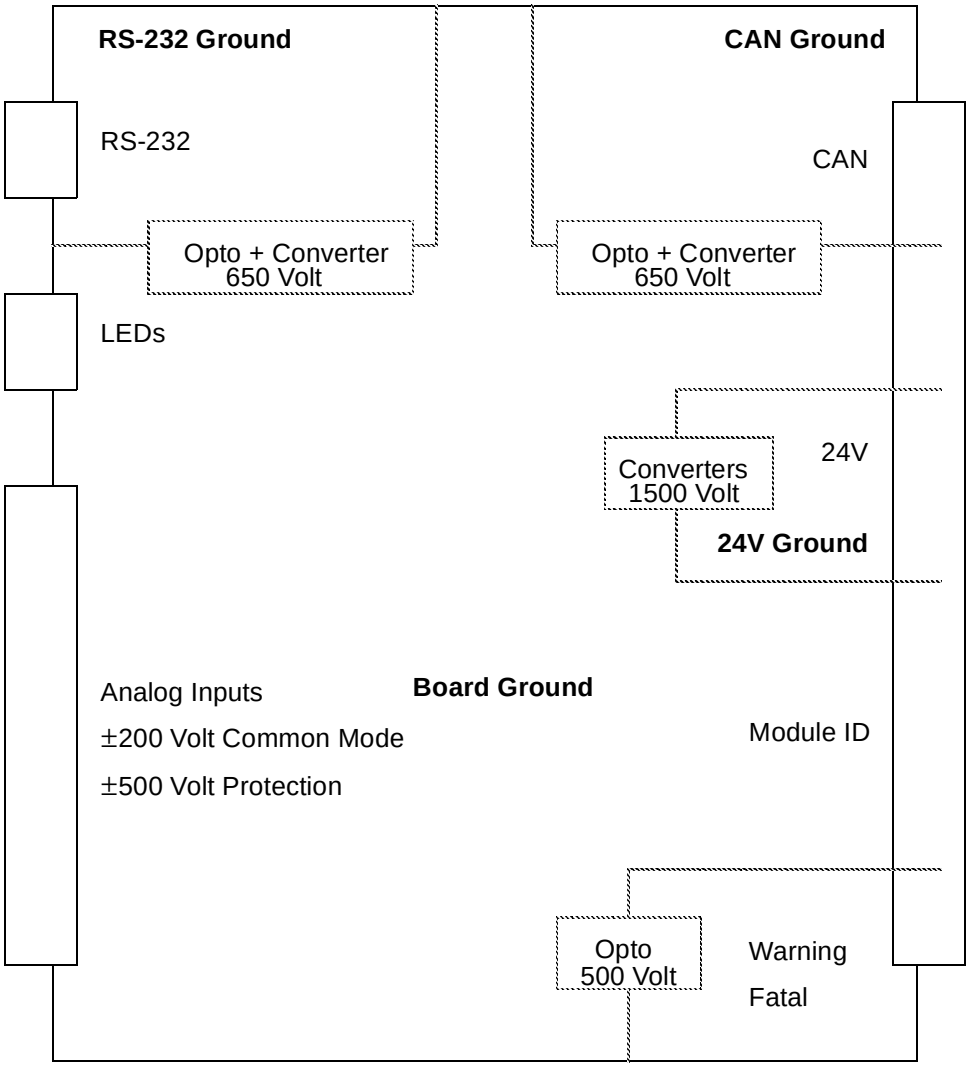

Figure A-2 Grounding Concept

Appendix B

Schematic Diagrams

1. Top Schematics
2. Input Voltages Connector
3. CAN Interface
4. DC/DC Converters and Decoupling
5. Microcontroller
6. Glue Logic
7. Miscellaneous
8. Bus Connector DIN-96
9. C515C Pin Assignments
10. Voltage Monitor
11. Voltage Monitor Group 0
12. Voltage Monitor Group 1
13. Voltage Monitor Group 2
14. Voltage Monitor Group 3
15. Voltage Monitor Group 4
16. Memory Devices
17. Module Number and Alarms
18. RS-232 Interface

Appendix C

Component Layout

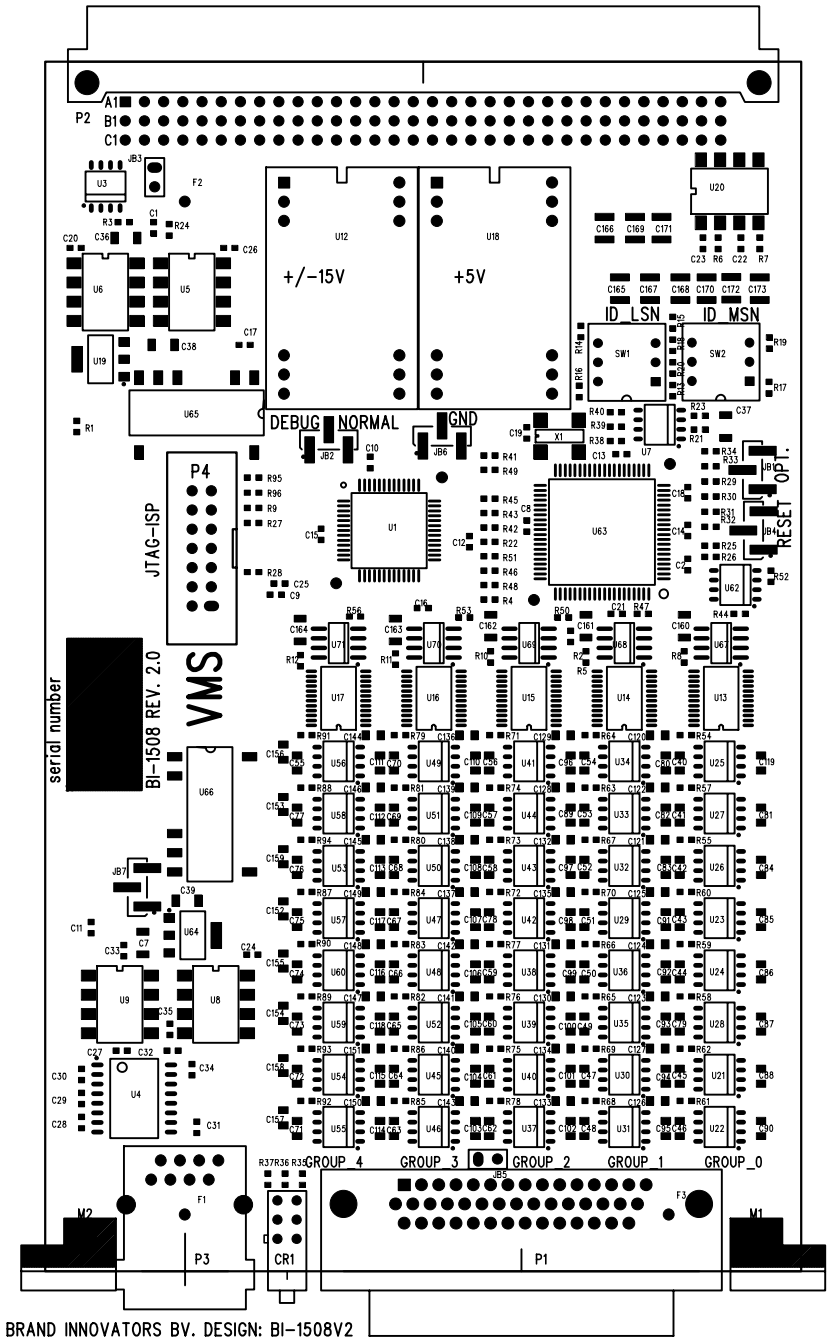

Figure C-1 Component Layout

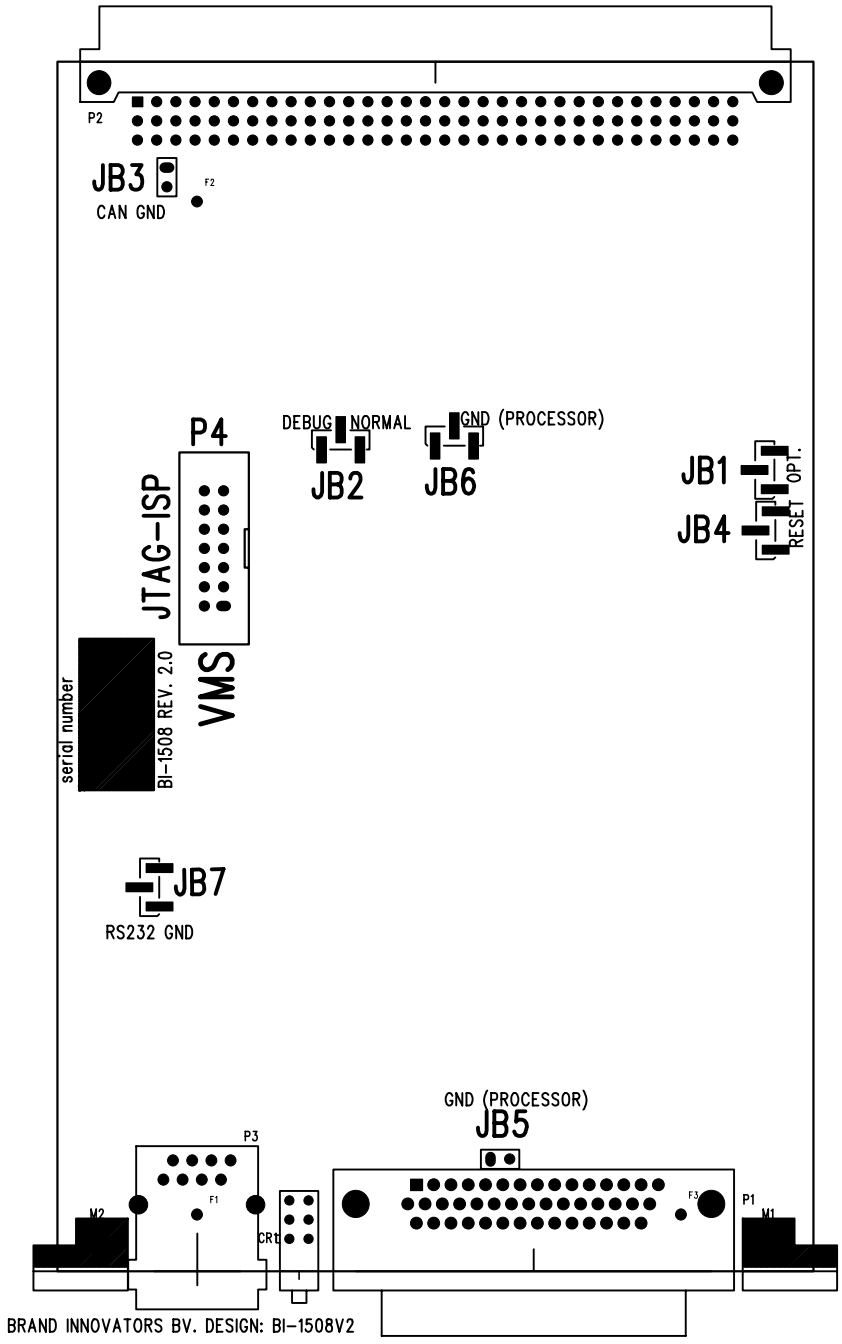

Figure C-2 Jumper Locations

Appendix D List of Components

Table D-1 List of Capacitors

Quantity	Reference Designator	Device	Value
1	C1	KKK11776	1NF
29	C2,C8-35	KKK4377	0.1UF
9	C7,C36,C38-39,C160-164	KKK6505	4.7UF
1	C37	KKK3913	1.0UF
120	C40-159	KKK4107	470NF
9	C165-173	KKK5472	22NF

Table D-2 List of Resistors

Quantity	Reference Designator	Device	Value
15	R1-2,R5,R8,R10-20	WRC10548	3K9
1	R3	CR10473JT	47K
26	R4,R9,R21-22,R26-28,R30,R34,R40-53,R56,R95-96	WRC6582	10K0
6	R6-7,R23,R35-37	WRC11606	330
2	R24-25	WRC9736	0
2	R29,R32	WRC6483	100K
43	R31,R33,R39,R54-55,R57-94	WRC6589	23K2
1	R38	WRC6300	18K0

Table D-3 List of Connectors and Jumpers

Quantity	Reference Designator	Device
1	P1	DDM-44DS-1059
1	P2	0-0650913-5
1	P3	SS6488SAFLS
1	P4	09185146324
4	JB1-2,JB4,JB6-7	0-0146128-1
2	JB3,JB5	SIP-2P

Table D-4 List of Integrated Circuits

Quantity	Reference Designator	Device
1	U1	PSD854F2-XXM
1	U3	PCA82C251T

Table D-4 List of Integrated Circuits

Quantity	Reference Designator	Device
1	U4	LT1181AISW
4	U5-6,U8-9	HCPL7710#300
1	U7	TL7702BID
1	U12	TEH2423
5	U13-17	LTC1598IG
1	U18	TEH2411
2	U19,U64	LT1121IST-5
2	U20	LH1522AAC
40	U21-60	AD629BR
1	U62	AT25040N-10SI
1	U63	SAF_C515C_LM
2	U65-66	DCP010505P-U
5	U67-71	LT1634AIS8-5

Table D-5 List of Oscillators

Quantity	Reference Designator	Device	Value
1	X1	SG8002CA-PHM-10MHZ	10MHZ

Table D-6 List of Miscellaneous Components

Quantity	Reference Designator	Device	Value
1	CR1	570-0100-132	R,G,Y
2	SW1-2	DRD16C	

Appendix E Connector Assignments

Table E-1 Analog Input Connector

Pin Number	Name	Pin Number	Name	Pin Number	Name
01	VI39	16	VI40		
02	VI36	17	VI37	31	VI38
03	VI33	18	VI34	32	VI35
04	VI30	19	VI31	33	VI32
05	VI27	20	VI28	34	VI29
06	VI24	21	VI25	35	VI26
07	VI21	22	VI22	36	VI23
08	GND	23	GND	37	GND
09	VI18	24	VI19	38	VI20
10	VI15	25	VI16	39	VI17
11	VI12	26	VI13	40	VI14
12	VI9	27	VI10	41	VI11
13	VI6	28	VI7	42	VI8
14	VI3	29	VI4	43	VI5
15	VI0	30	VI1	44	VI2

Table E-2 RS-232 Connector

Pin number	Name	Direction
1	-	-
2	Receive Data	In
3	Transmit Data	Out
4	-	-
5	RS-232 Ground	-
6	-	-
7	-	-
8	-	-

Table E-3 DIN-96 Pinning

Pin Number	Name	Pin Number	Name	Pin Number	Name
A01	CAN_H	B01	-	C01	CAN_L
A02	CAN_GND	B02	-	C02	CAN_GND
A03	-	B03	-	C03	-
A04	-	B04	-	C04	-
A05	-	B05	-	C05	-
A06	-	B06	-	C06	-
A07	24VPOS	B07	-	C07	24VNEG
A08	24VPOS	B08	-	C08	24VNEG
A09	24VPOS	B09	-	C09	24VNEG
A10	24VPOS	B10	-	C10	24VNEG
A11	24VPOS	B11	-	C11	24VNEG
A12	-	B12	-	C12	-
A13	-	B13	-	C13	-
A14	-	B14	-	C14	-
A15	-	B15	-	C15	-
A16	-	B16	-	C16	-
A17	-	B17	-	C17	-
A18	MODP0	B18	-	C18	MODM0
A19	MODP1	B19	-	C19	MODM1
A20	MODP2	B20	-	C20	MODM2
A21	MODP3	B21	-	C21	MODM3
A22	MODP4	B22	-	C22	MODM4
A23	MODP5	B23	-	C23	MODM5
A24	MODP6	B24	-	C24	MODM6
A25	MODP7	B25	-	C25	MODM7
A26	-	B26	-	C26	-
A27	-	B27	-	C27	-
A28	-	B28	-	C28	-
A29	-	B29	-	C29	-
A30	FATAL0	B30	-	C30	FATAL1
A31	-	B31	-	C31	-
A32	WARNING0	B32	-	C32	WARNING1

Table E-4 In System Programming

Pin Number	Name	Description
1	$\overline{\text{JEN}}$	JTAG Enable, No Connect
2	$\overline{\text{TRST}}$	JTAG Reset, No Connect

Table E-4 In System Programming

Pin Number	Name	Description
3	GND	Device Ground
4	CNTL	No Connect
5	TDI	JTAG Data to Device
6	TSTAT	JTAG Status
7	VCC	Device Power
8	$\overline{\text{RST}}$	Device Reset
9	TMS	JTAG State Machine Control
10	GND	Device Ground
11	TCK	JTAG Clock
12	GND	Device Ground
13	TDO	JTAG Data from Device
14	$\overline{\text{TERR}}$	JTAG Error

Appendix F Memory Map

The following table gives the address map for the BI-1508.

Table F-1 Memory Map

Address	Code Space	Data Space
FFFF ... F800	Main Flash Segment 0 32k bytes	Internal XRAM 2k bytes
F7FF ... F700		Internal CAN Controller 256 bytes
F0FF ... F000		CSIOP in PSD device 256 bytes
EFFF ... A000		not used
9FFF ... 8000		
7FFF ... 6000	not used	SRAM in PSD device 32k bytes
5FFF ... 4000	Boot Flash Segment 2 8k bytes	
3FFF ... 2000	Boot Flash Segment 1 8k bytes	
1FFF ... 0000	Boot Flash Segment 0 8k bytes	

The following table gives the address map for the BI-1508 when the monitor mode is selected. The baudrate of the monitor is self-adjusting, with a maximum of 57600 baud.

Table F-2 Memory Map (Monitor Mode)

<table>
<tr><th>Address</th><th>Code Space</th><th>Data Space</th></tr>
<tr><td>FFFF
...
F800</td><td rowspan="5">not used</td><td>Internal XRAM
2k bytes</td></tr>
<tr><td>F7FF
...
F700</td><td>Internal CAN Controller
256 bytes</td></tr>
<tr><td>F0FF
...
F000</td><td>CSIOP in PSD device
256 bytes</td></tr>
<tr><td>EFFF
...
A000</td><td rowspan="2">not used</td></tr>
<tr><td>9FFF
...
8000</td><td>Boot Flash Segment 3
8k bytes
Monitor code</td></tr>
<tr><td>7FFF
...
7F00</td><td colspan="2">Monitor xdata</td></tr>
<tr><td>7EFF
...
6000</td><td colspan="2" rowspan="4">SRAM in PSD device
32k bytes
Free for user code and xdata</td></tr>
<tr><td>5FFF
...
4000</td></tr>
<tr><td>3FFF
...
2000</td></tr>
<tr><td>1FFF
...
0000</td></tr>
</table>

Appendix G Mechanical Specifications

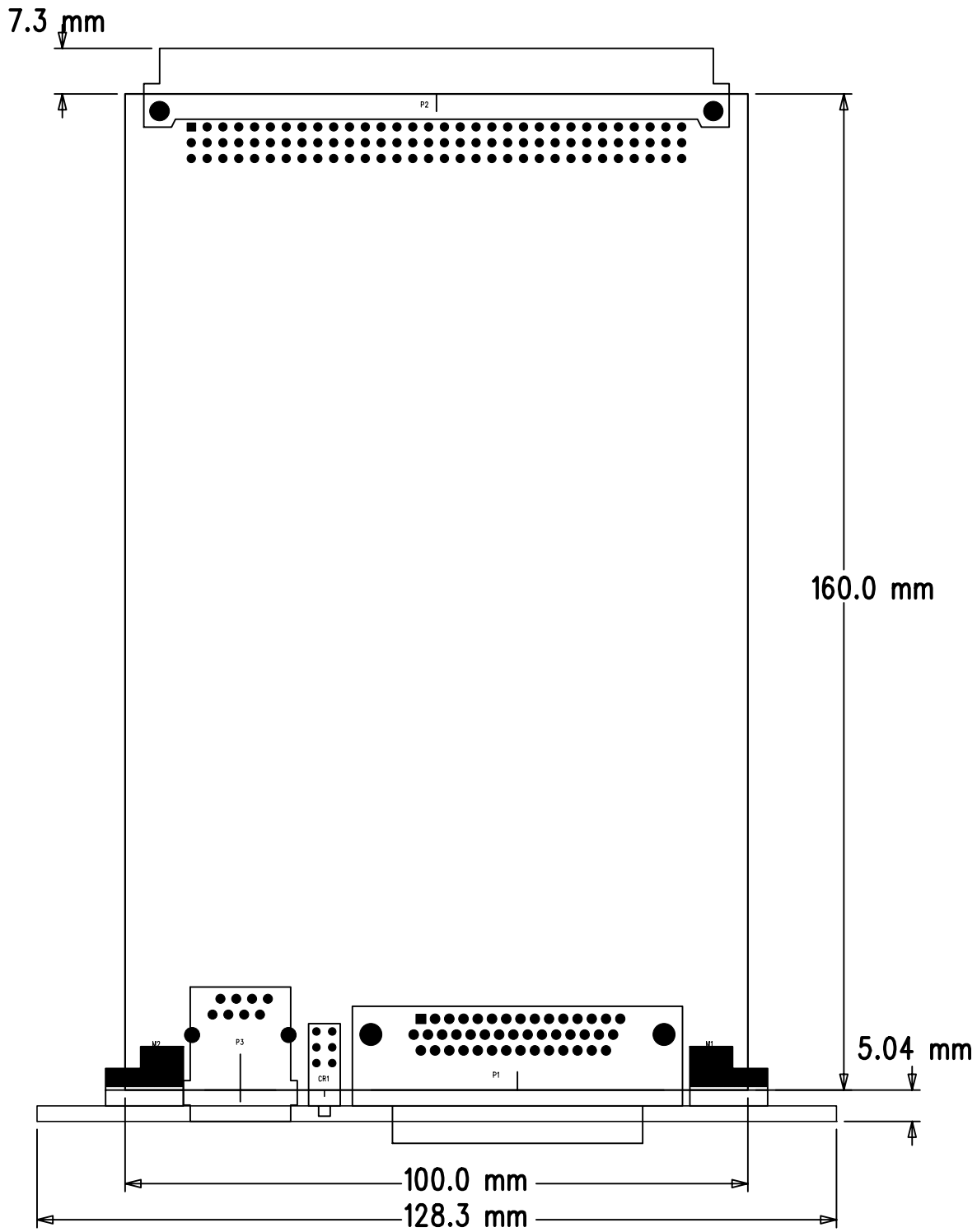

Figure G-1 Mechanical Specifications

Appendix H Application Notes

Available software:

- Read the 40 ADC inputs
- Read the three supply inputs
- Read the Module ID registers
- Read and modify the EEPROM using SPI
- Send and receive through RS-232
- Send and receive through CAN