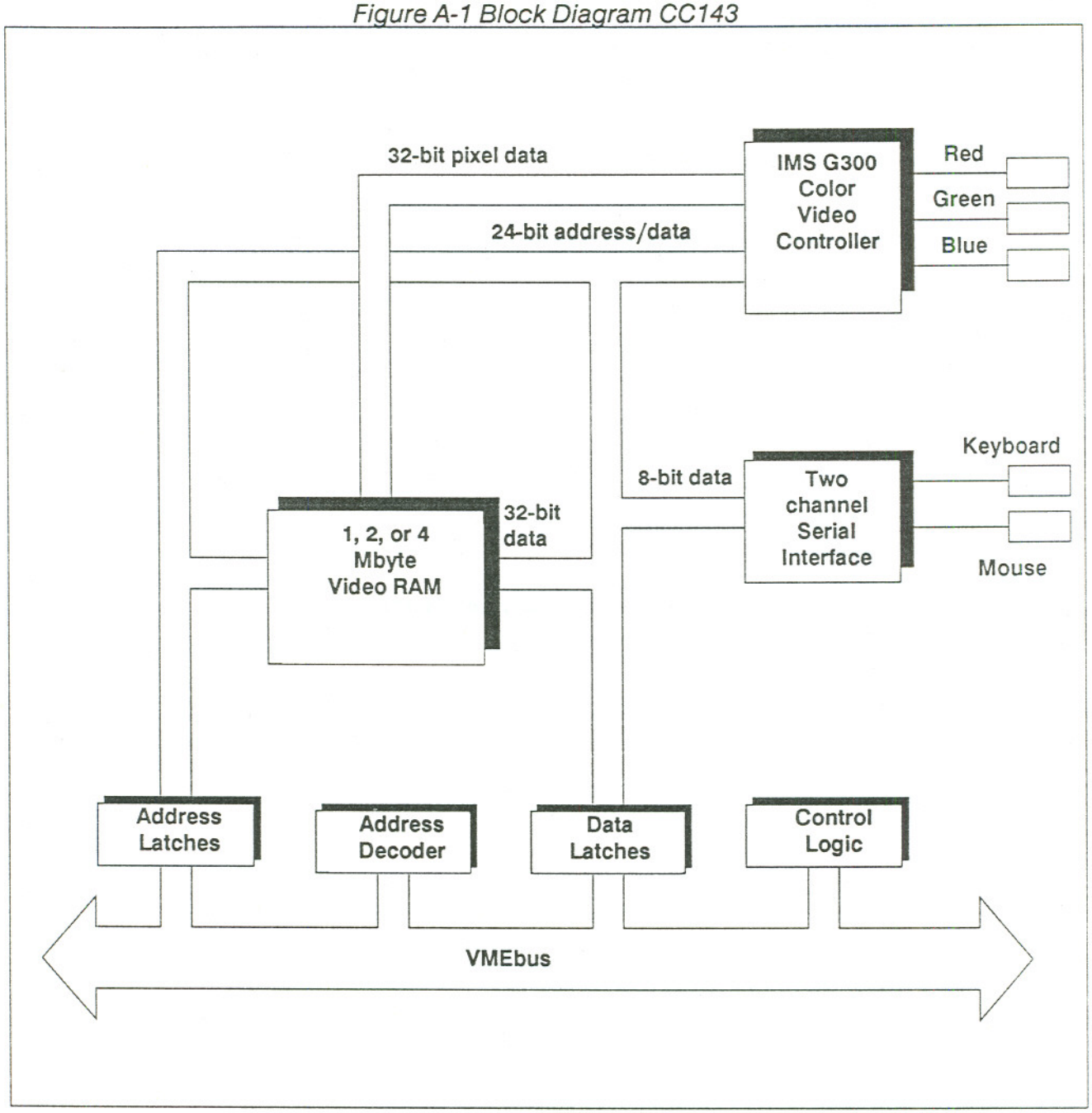
Appendix A Block Diagram

Figure A-1 Block Diagram CC143



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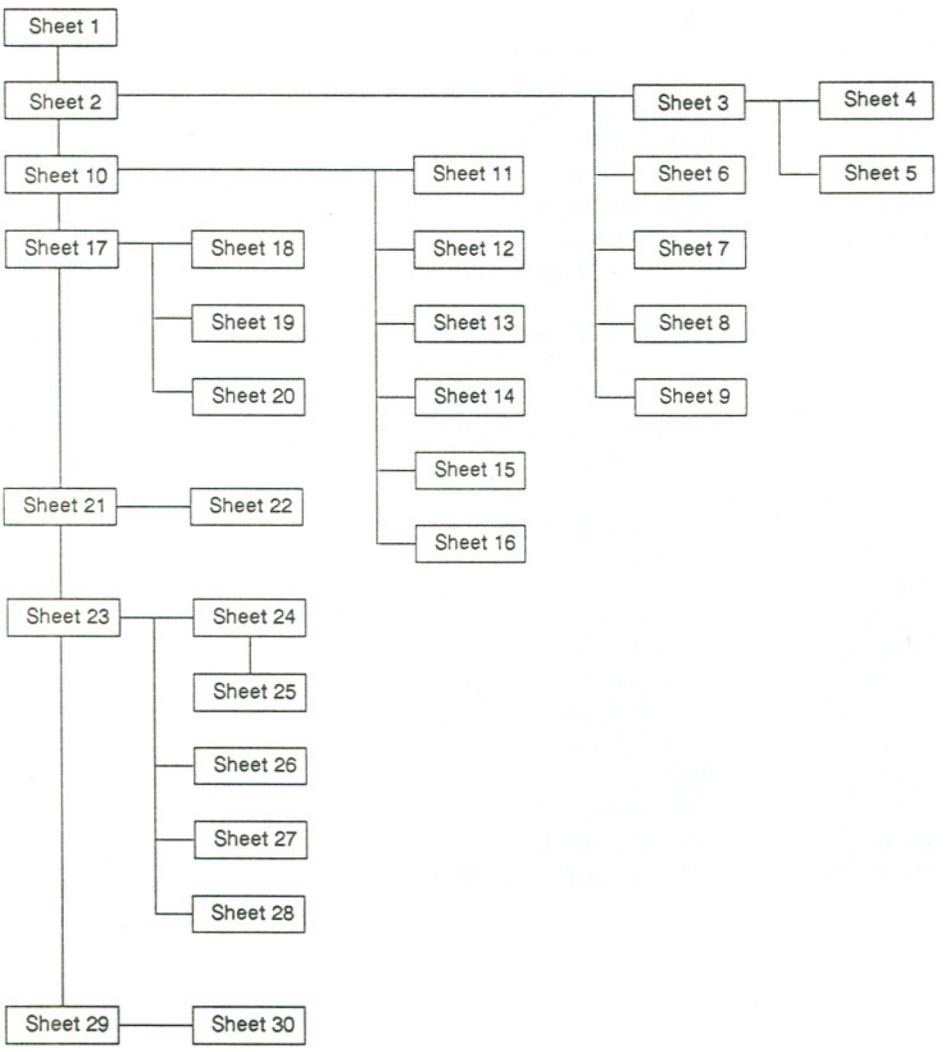
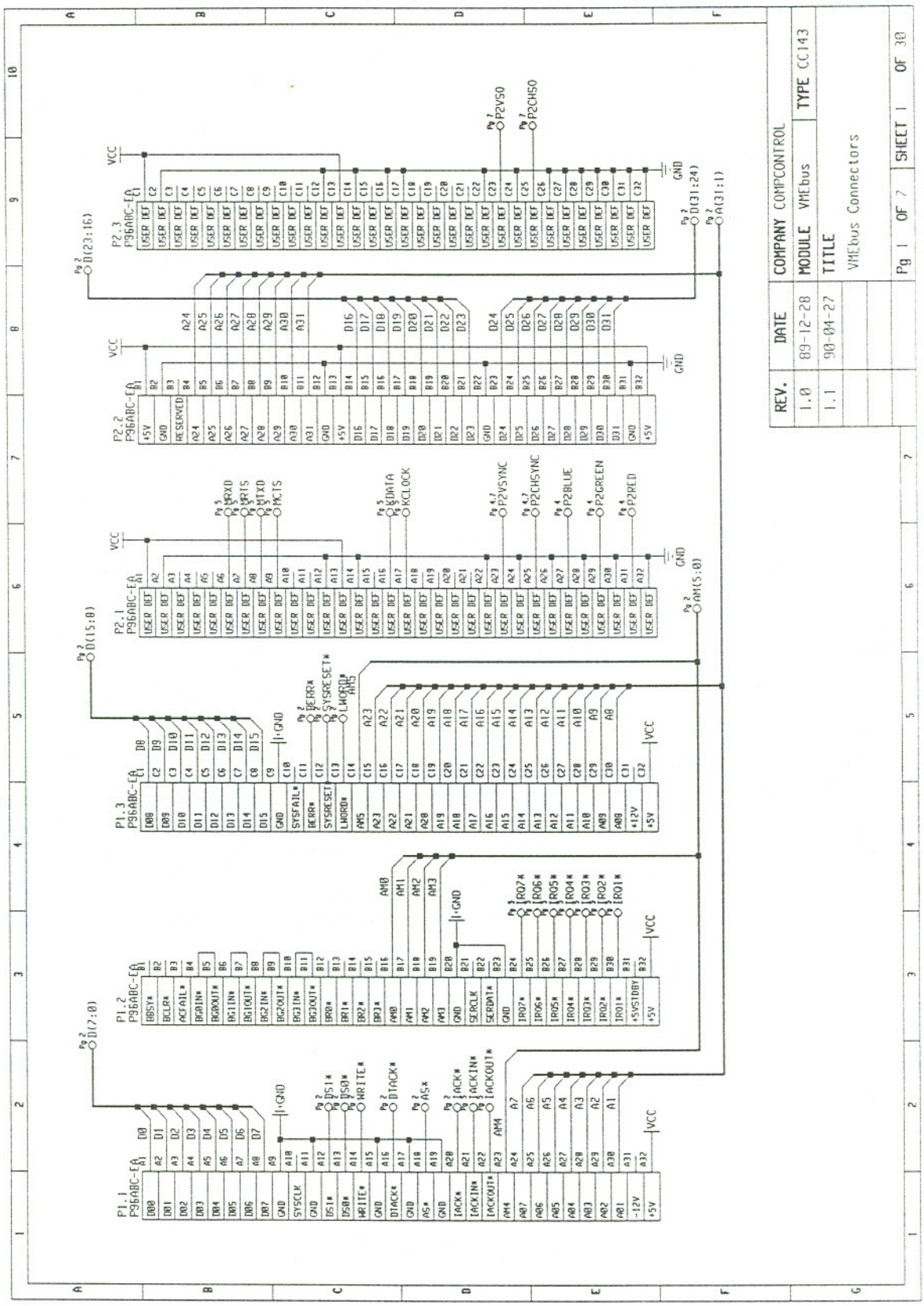
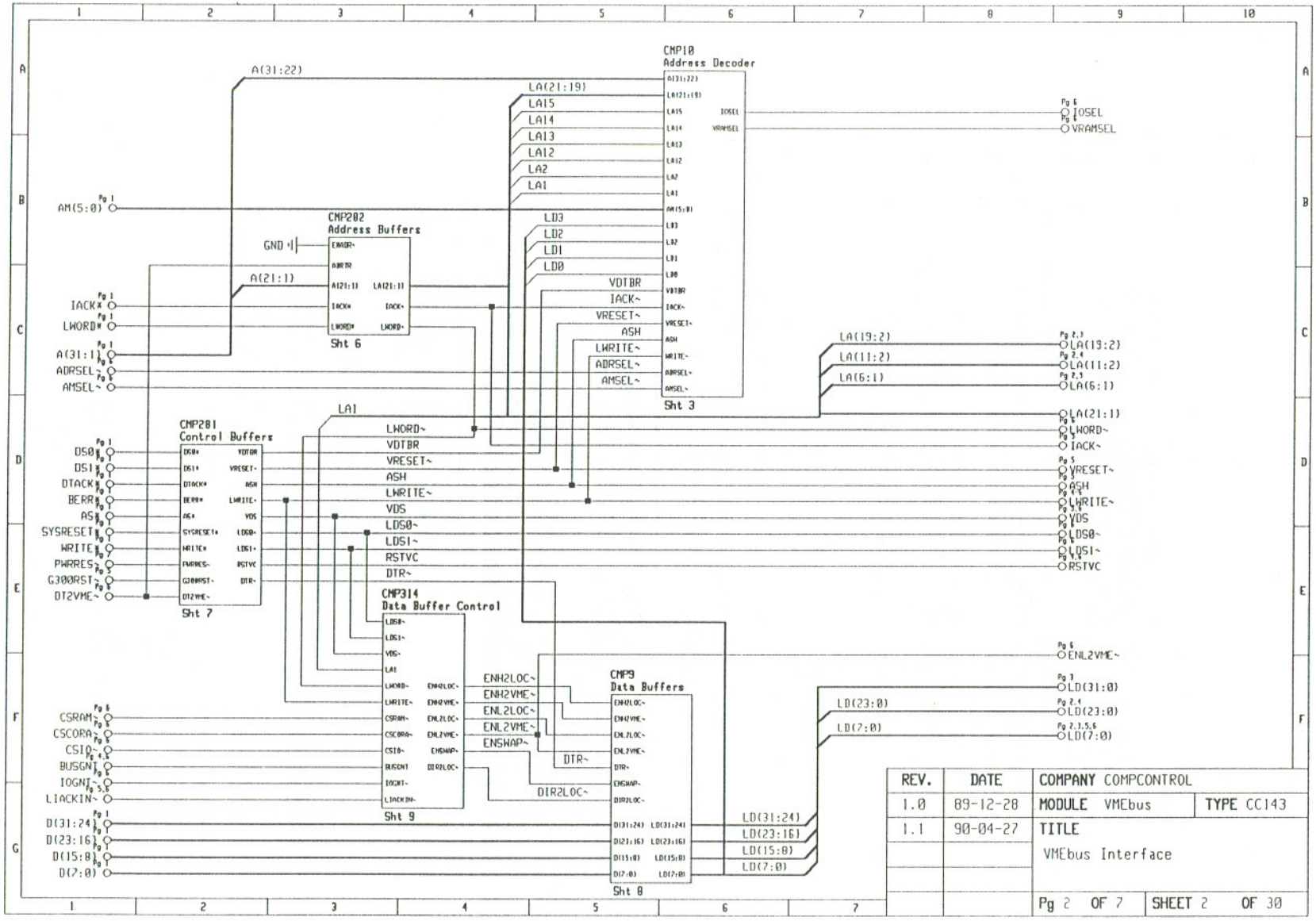
Appendix B Schematic Diagrams

Sheet Hierarchy




REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE VMEbus Connectors
Pg 1 OF 7 SHEET 1 OF 30
P1.1 P96ABC-EA
P1.2 P96ABC-EA
P1.3 P96ABC-EA
P2.1 P96ABC-EA
P2.2 P96ABC-EA
P2.3 P96ABC-EA
D(7:0)
D(15:0)
D(23:16)
D(31:24)
A(31:1)
A(15:0)
VCC
GND
SYSCLK
DS1*
DS0*
WRITE*
DTACK*
AS*
IACK*
IACKIN*
IACKOUT*
AM4
AM5
AM0
AM1
AM2
AM3
IRQ7*
IRQ6*
IRQ5*
IRQ4*
IRQ3*
IRQ2*
IRQ1*
SYSFAIL*
BERR*
SYSRESET*
LWORD*
MRXD
MRTS
MTXD
MCTS
KDATA
KCLOCK
P2VSYNC
P2CHSYNC
P2BLUE
P2GREEN
P2RED
P2V50
P2CH50



REV.	DATE	COMPANY COMPCONTROL	
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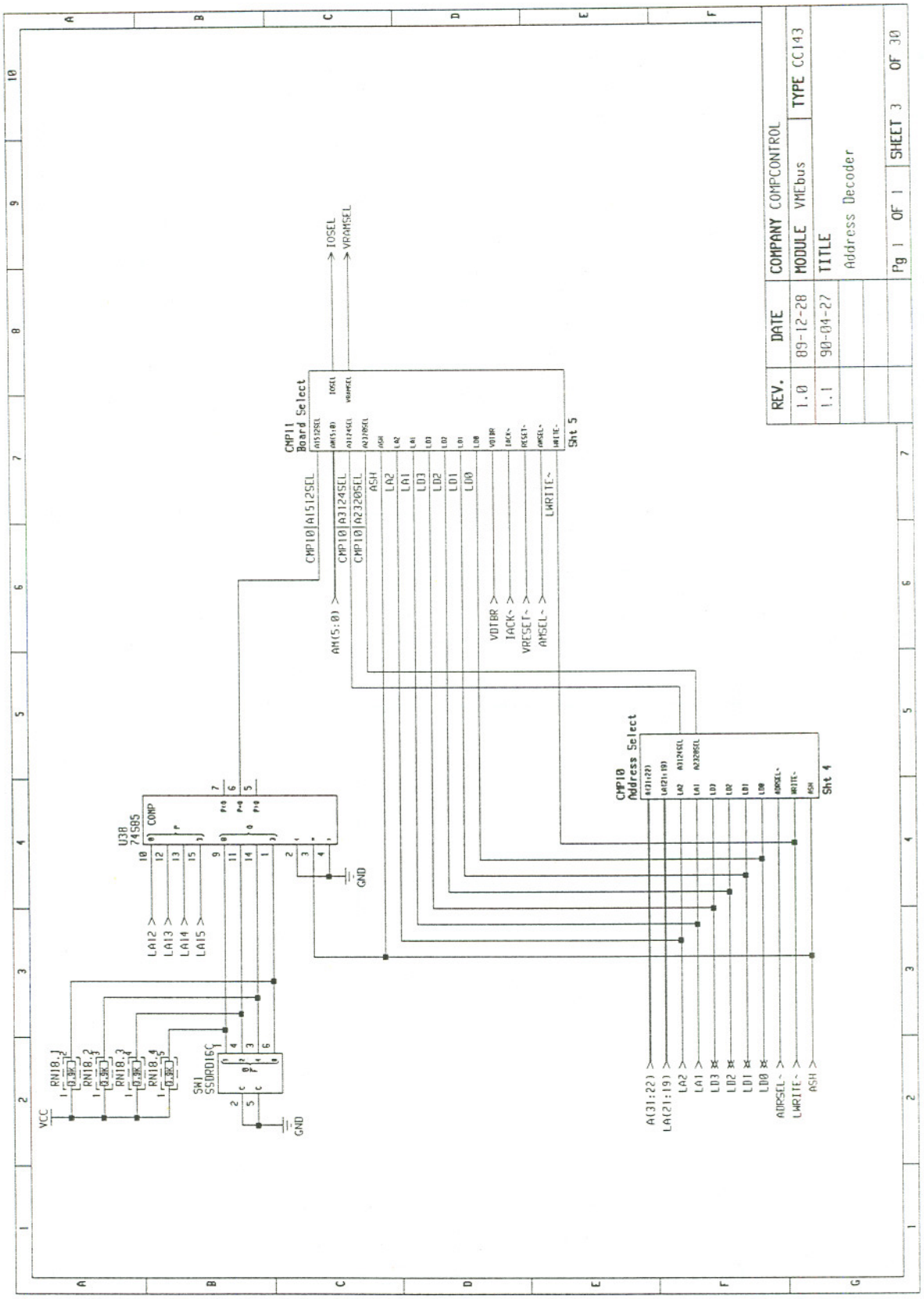
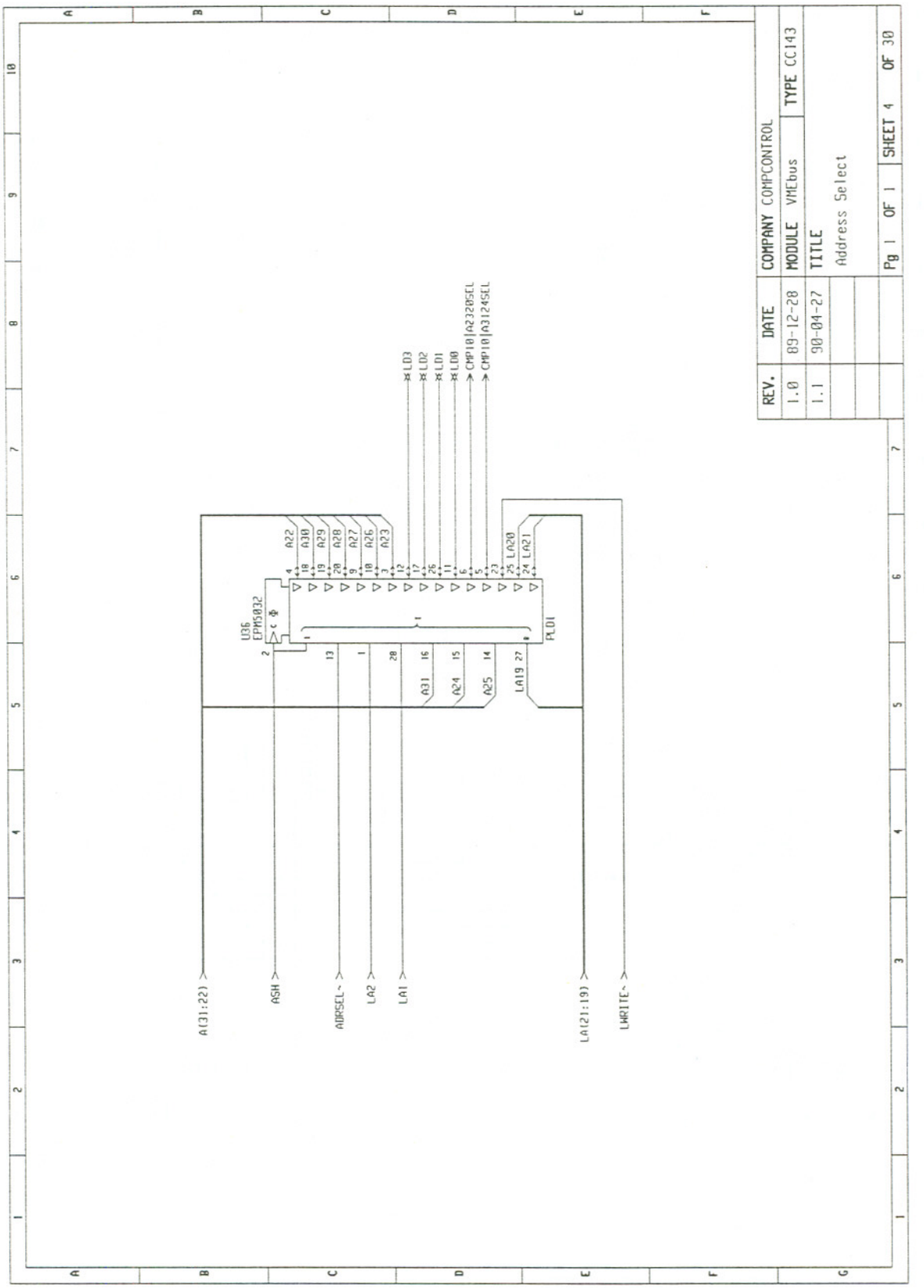
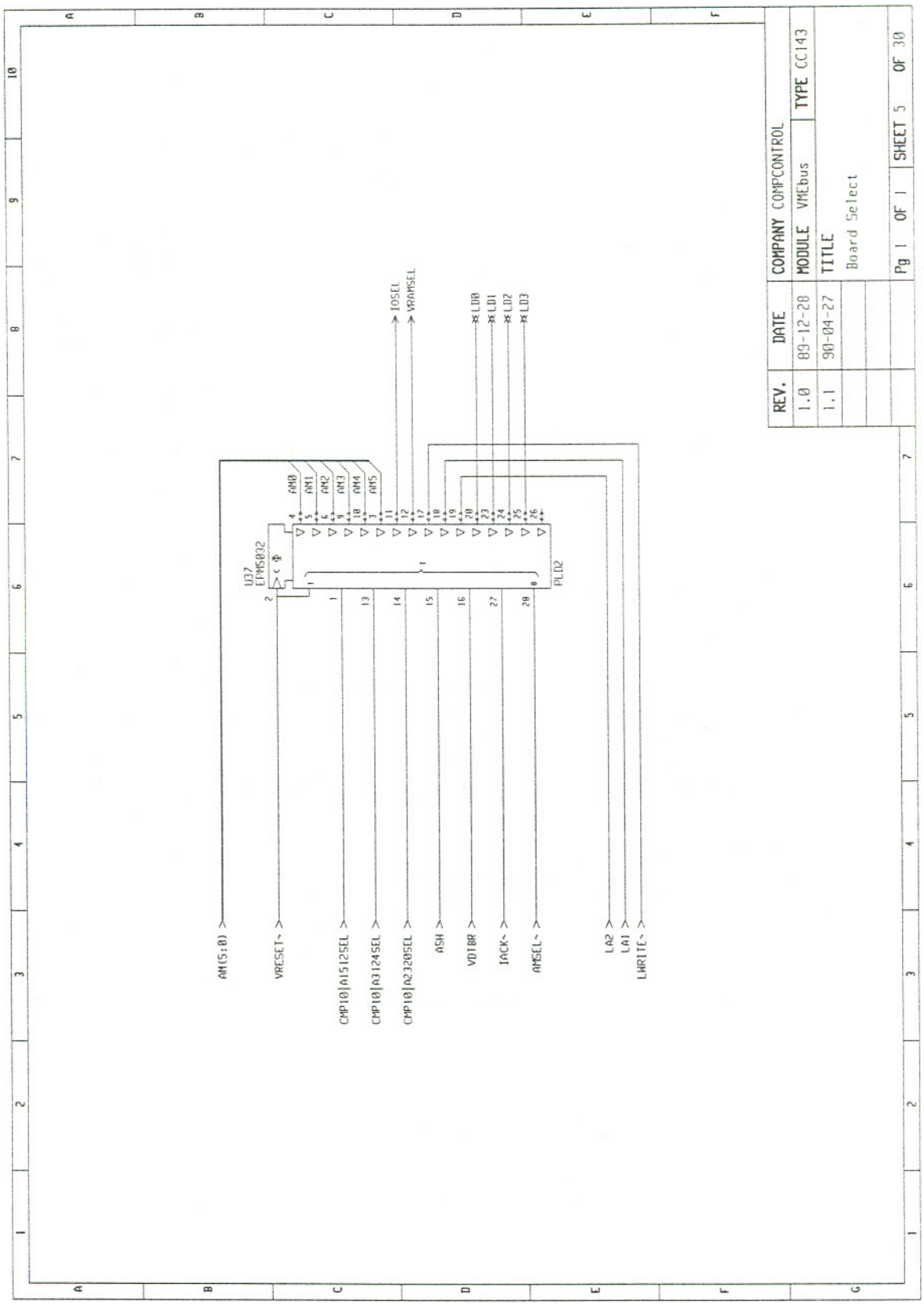
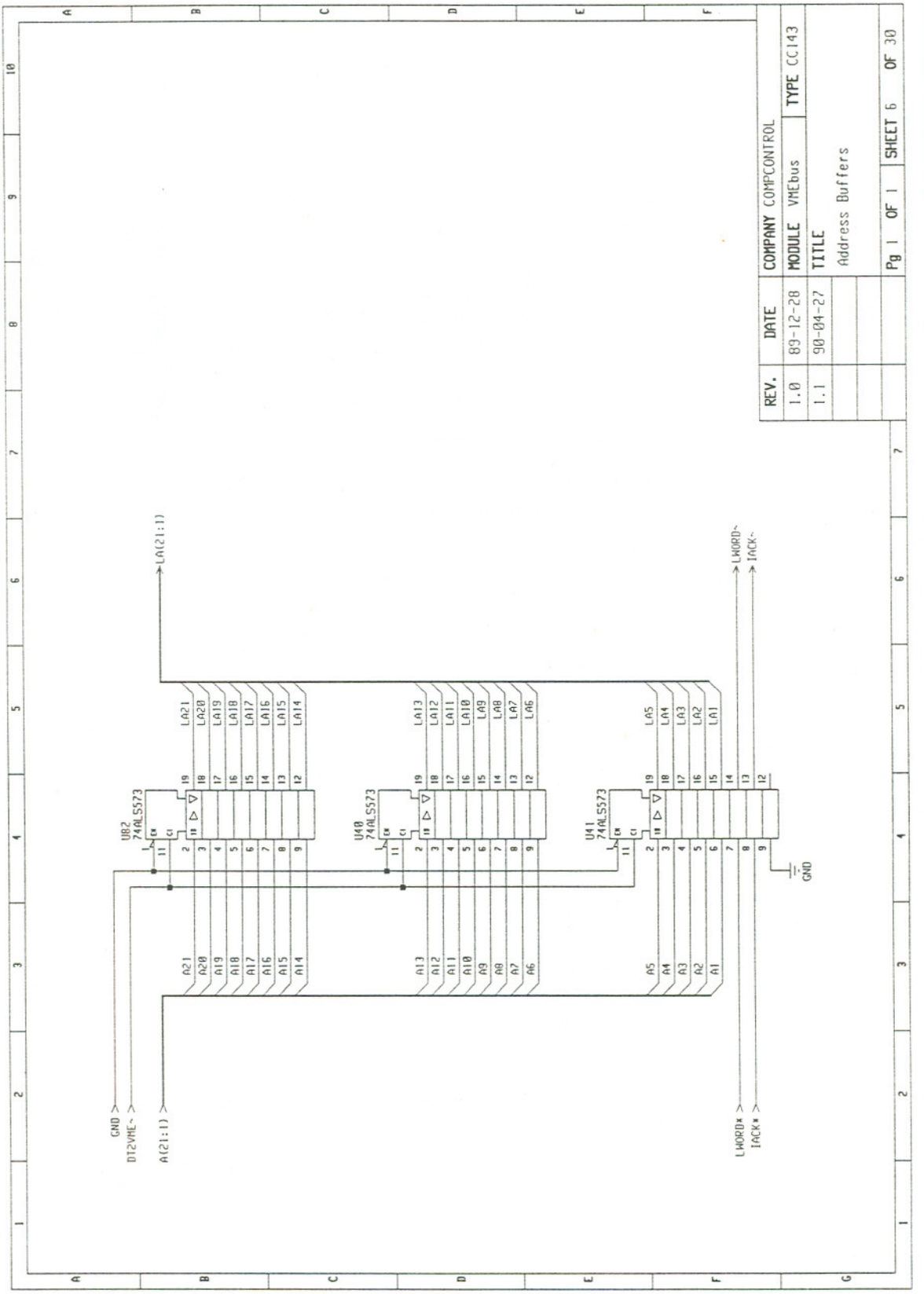
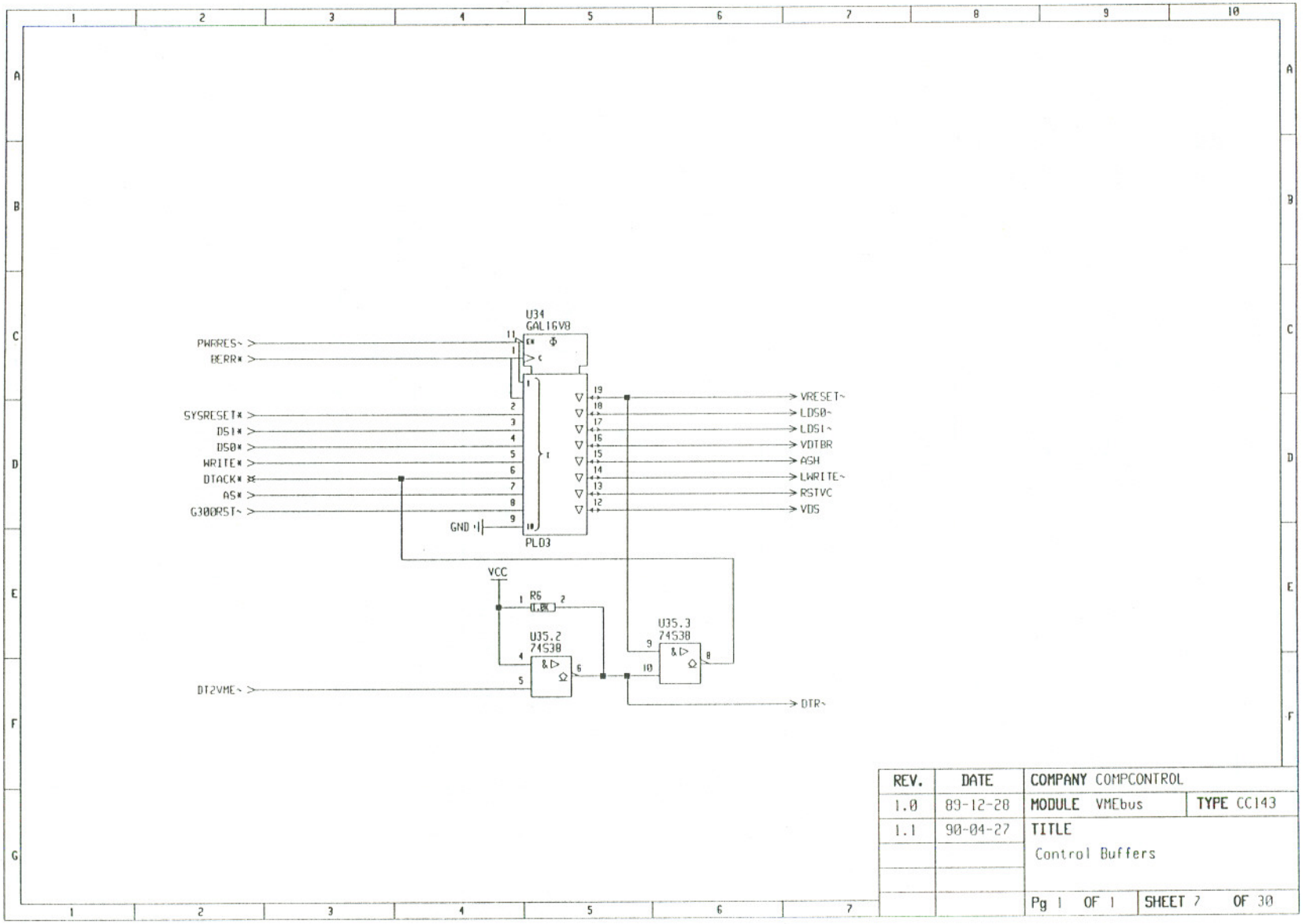
1.1	90-04-27	TITLE VMEbus Interface	
		Pg 2 OF 7	SHEET 2 OF 30


REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
Address Decoder
Pg 1 OF 1
SHEET 3 OF 30
CMP11 Board Select
Sht 5
CMP10 Address Select
Sht 4
U38 74S85 COMP
SW1 SSORD16C
RN18.1
RN18.2
RN18.3
RN18.4
RN18.5
VCC
GND
IOSEL
VRAMSEL
AM(5:0)
VDTBR
IACK~
VRESET~
AMSEL~
LWRITE~
LA12
LA13
LA14
LA15
A(31:22)
LA(21:19)
LA2
LA1
LD3
LD2
LD1
LD0
ADRSEL~
ASH


REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE Address Select
Pg 1 OF 1 SHEET 4 OF 30
U36 EPM5032
A22 A30 A29 A28 A27 A26 A23
LD3 LD2 LD1 LD0
CMP10|A2320SEL
CMP10|A3124SEL
LA20 LA21
PLD1
A31 A24 A25 LA19
A(31:22)
ASH
ADRSEL~
LA2
LA1
LA(21:19)
LWRITE~


REV. | DATE | COMPANY COMPCONTROL
1.0 | 89-12-28 | MODULE VMEbus | TYPE CC143
1.1 | 90-04-27 | TITLE Board Select
Pg 1 OF 1 | SHEET 5 OF 30
IOSEL
VRAMSEL
LD0
LD1
LD2
LD3
AM0
AM1
AM2
AM3
AM4
AM5
U37
EPM5032
PLD2
AM(5:0)
VRESET~
CMP10|A1512SEL
CMP10|A3124SEL
CMP10|A2320SEL
ASH
VDTBR
IACK~
AMSEL~
LA2
LA1
LWRITE~


COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
Address Buffers
Pg 1 OF 1
SHEET 6 OF 30
REV. DATE
1.0 89-12-28
1.1 90-04-27
LA(21:1)
LWORD~
IACK~
U02 74ALS573
U40 74ALS573
U41 74ALS573
GND
GND
DT2VME~
A(21:1)
LWORD*
IACK*



REV.	DATE	COMPANY COMPCONTROL	
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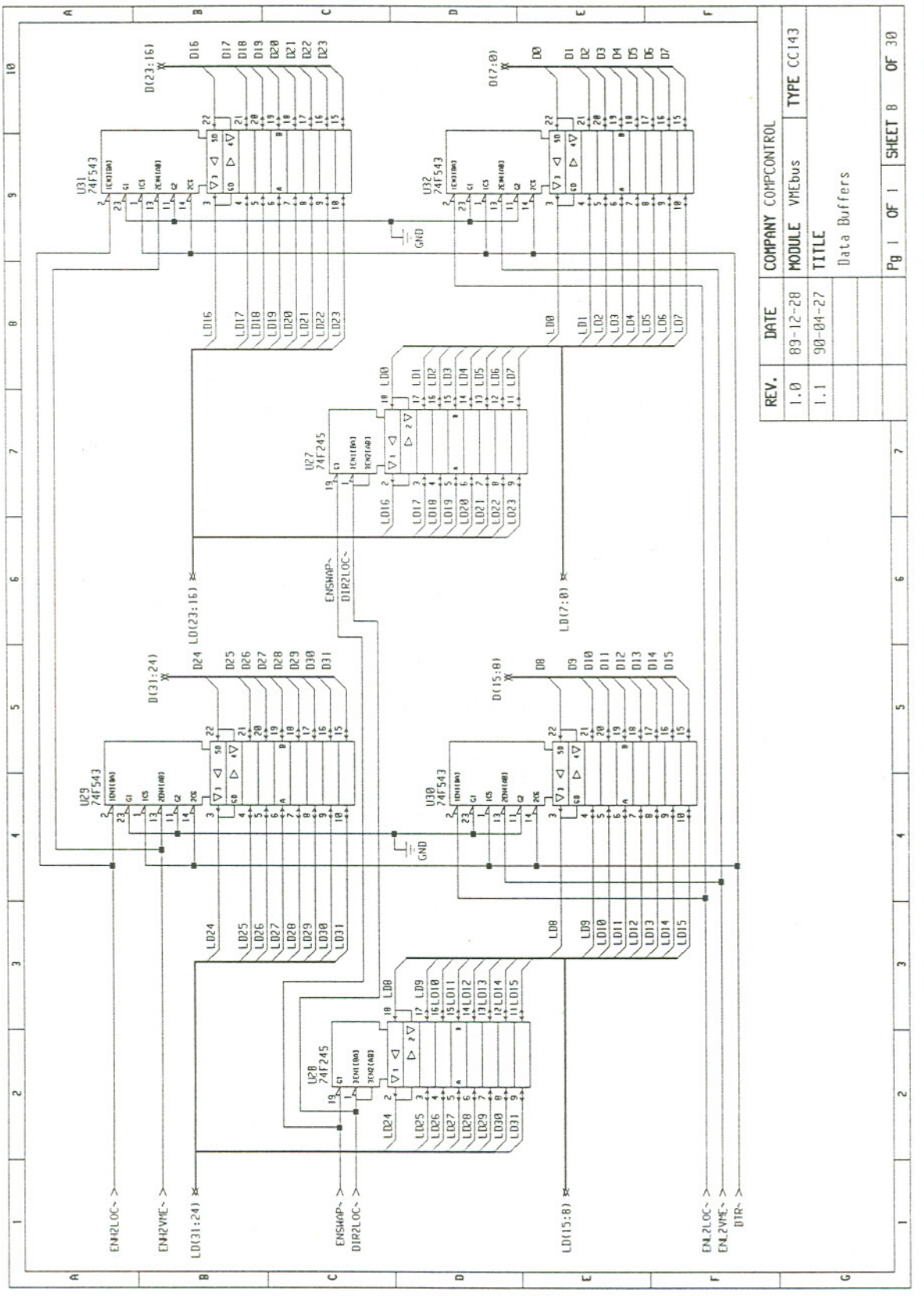
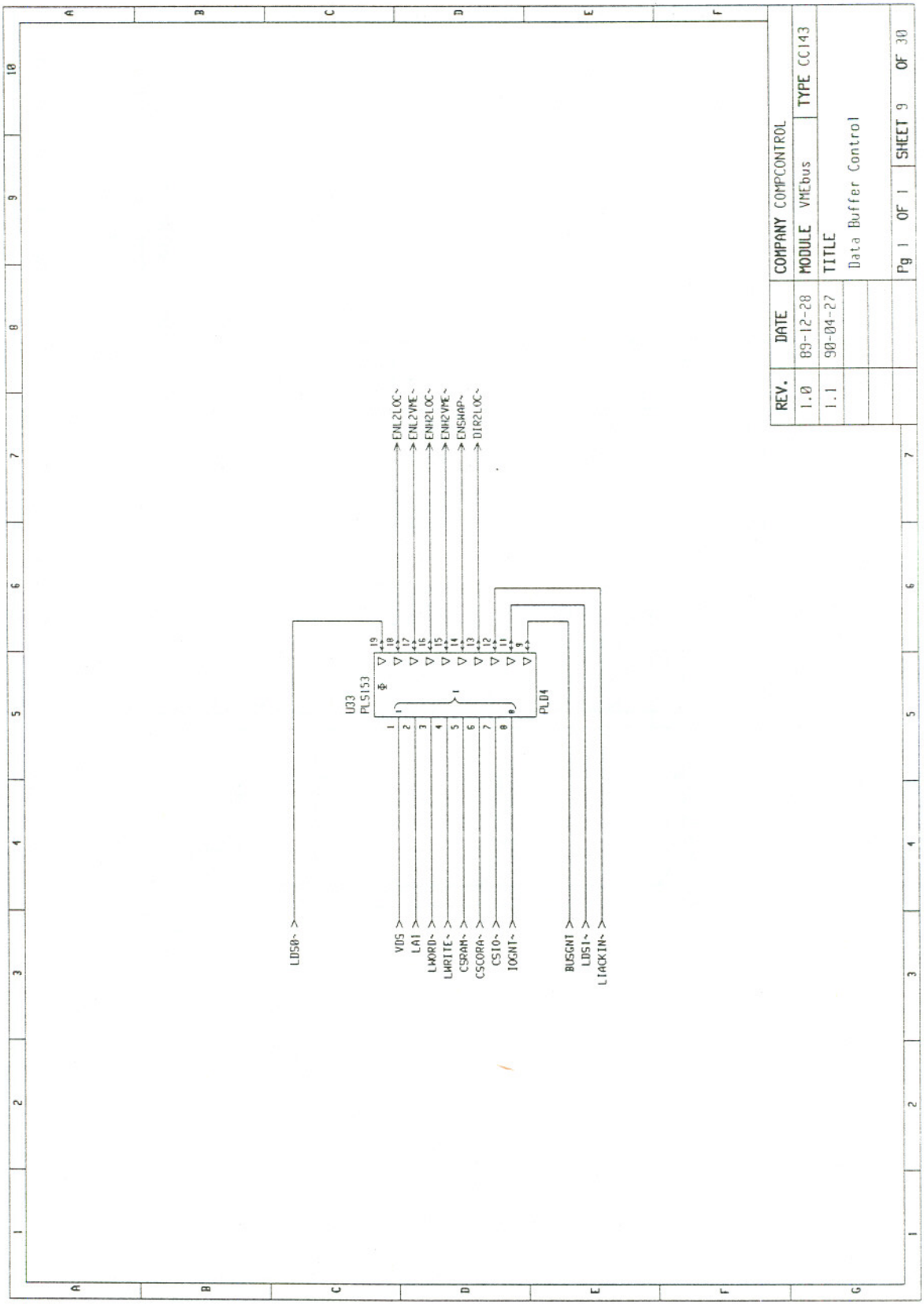
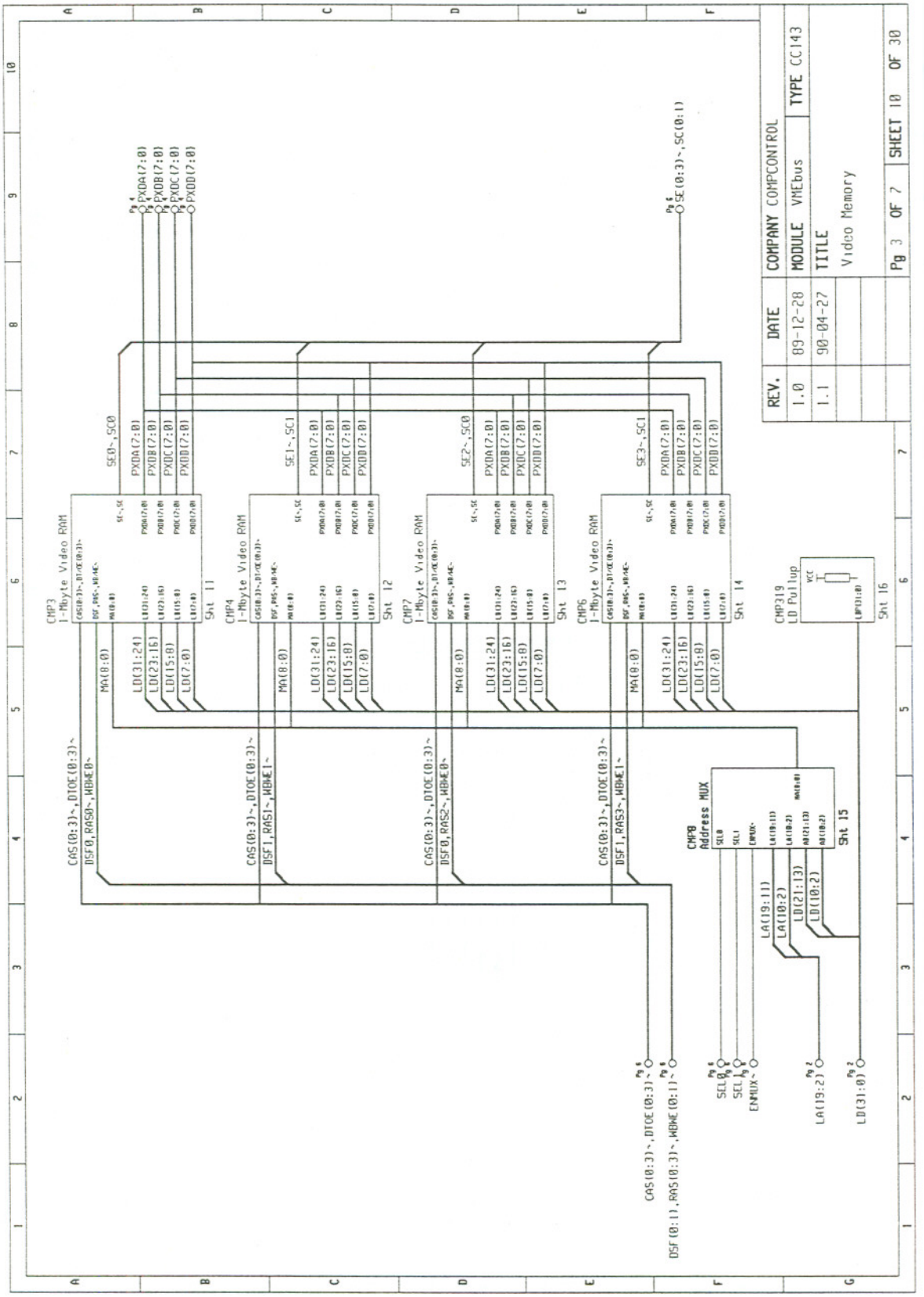
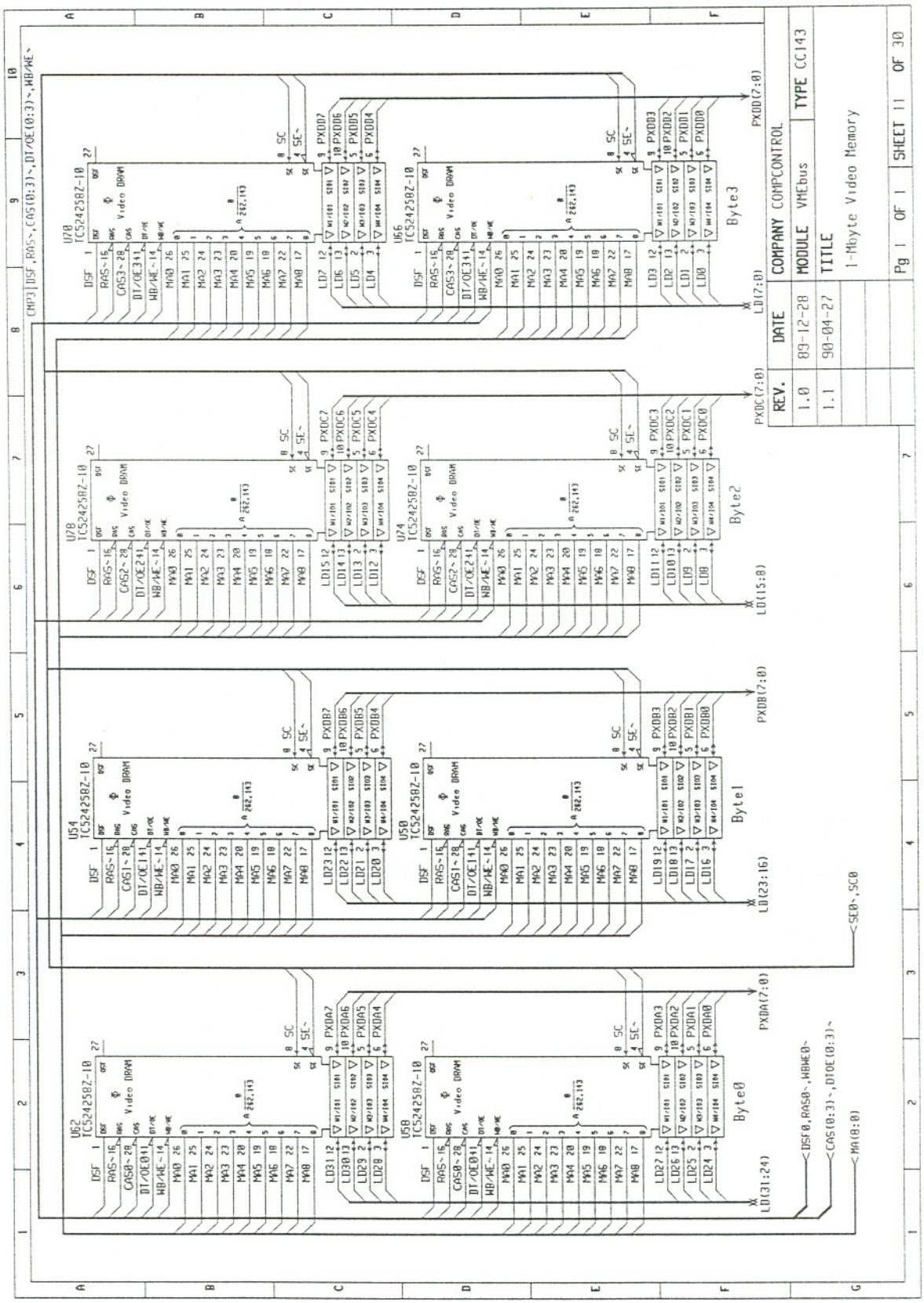
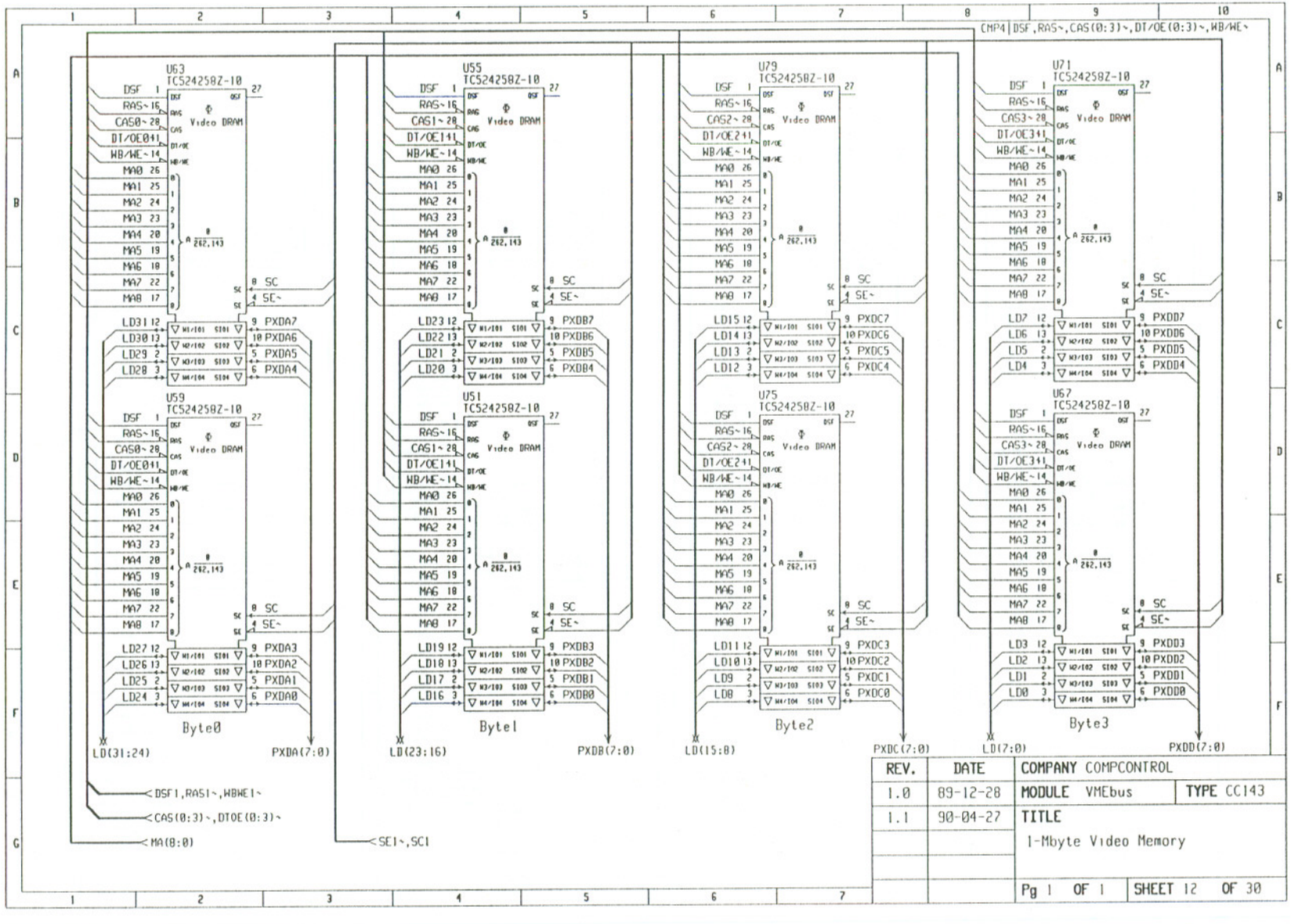
1.1	90-04-27	TITLE	
		Control Buffers	
		Pg 1 OF 1	SHEET 7 OF 30

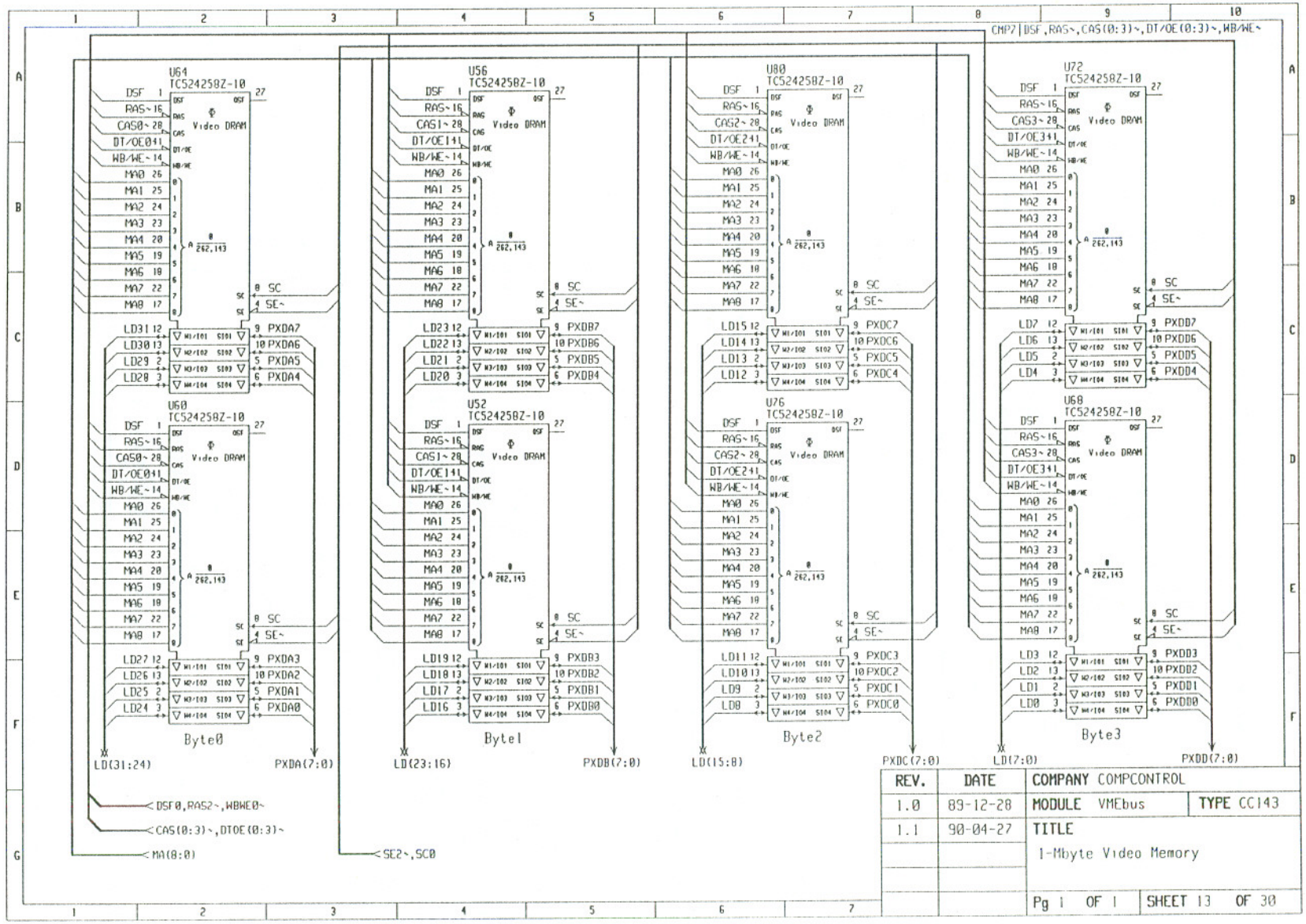

COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE Data Buffers
Pg 1 OF 1
SHEET 8 OF 30
REV. DATE
1.0 89-12-20
1.1 90-04-27
U31 74F543
U32 74F543
U29 74F543
U30 74F543
U27 74F245
U28 74F245
GND
D(23:16)
D(7:0)
D(31:24)
D(15:8)
LD(23:16)
LD(7:0)
LD(31:24)
LD(15:8)
ENSNAP~
DIR2LOC~
EN2LOC~
EN2VME~
DIR~
EN_2LOC~
EN_2VME~

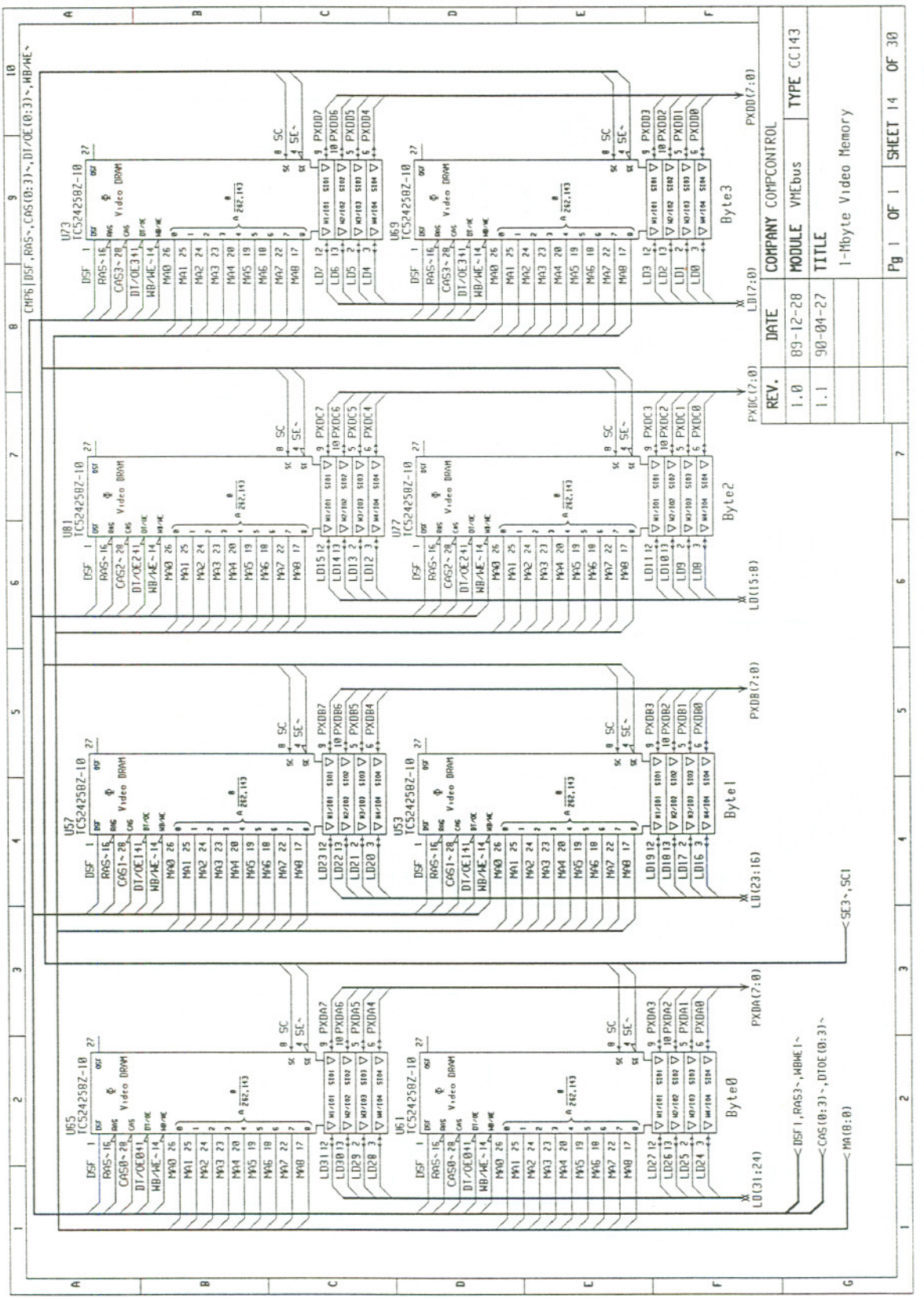

ENL2LOC~
ENL2VME~
ENH2LOC~
ENH2VME~
ENSWAP~
DIR2LOC~
U33
PLS153
PLD4
LD50~
VDS
LAI
LWORD~
LWRITE~
CSRAM~
CSCORA~
CS10~
IOGNT~
BUSGNT
LDS1~
LIACKIN~
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
Data Buffer Control
Pg 1 OF 1
SHEET 9 OF 30

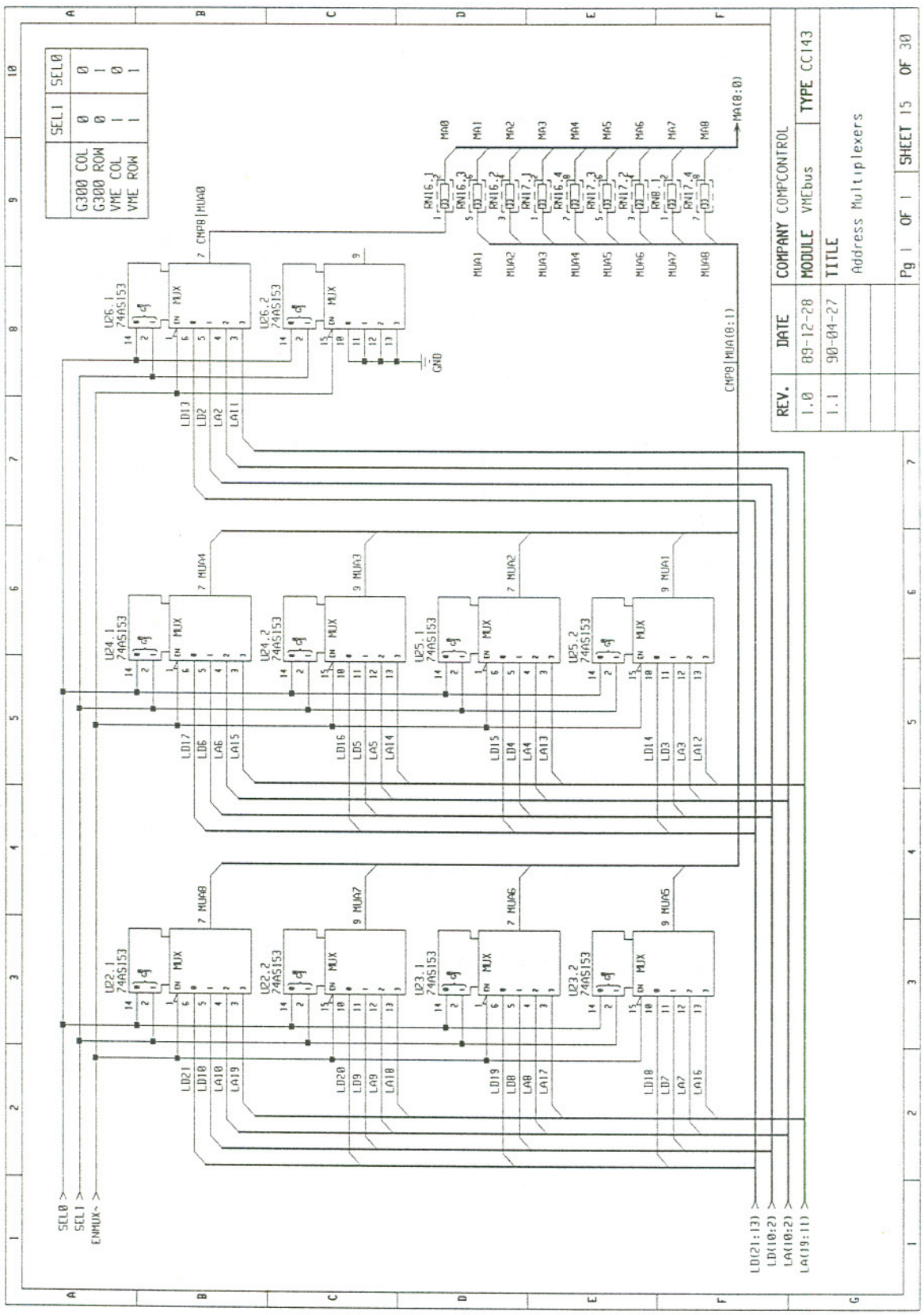

CMP3
1-Mbyte Video RAM
CMP4
1-Mbyte Video RAM
CMP7
1-Mbyte Video RAM
CMP6
1-Mbyte Video RAM
CMP8
Address MUX
CMP319
LD Pullup
SE0~,SC0
SE1~,SC1
SE2~,SC0
SE3~,SC1
PXDA(7:0)
PXDB(7:0)
PXDC(7:0)
PXDD(7:0)
MA(8:0)
LD(31:24)
LD(23:16)
LD(15:8)
LD(7:0)
CAS(0:3)~,DTOE(0:3)~
DSF0,RAS0~,WBWE0~
DSF1,RAS1~,WBWE1~
DSF0,RAS2~,WBWE0~
DSF1,RAS3~,WBWE1~
LA(19:11)
LA(10:2)
LD(21:13)
LD(10:2)
SEL0
SEL1
ENMUX~
Sht 11
Sht 12
Sht 13
Sht 14
Sht 15
Sht 16
SE(0:3)~,SC(0:1)
CAS(0:3)~,DTOE(0:3)~
DSF(0:1),RAS(0:3)~,WBWE(0:1)~
LA(19:2)
LD(31:0)
REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
Video Memory
Pg 3 OF 7
SHEET 10 OF 30

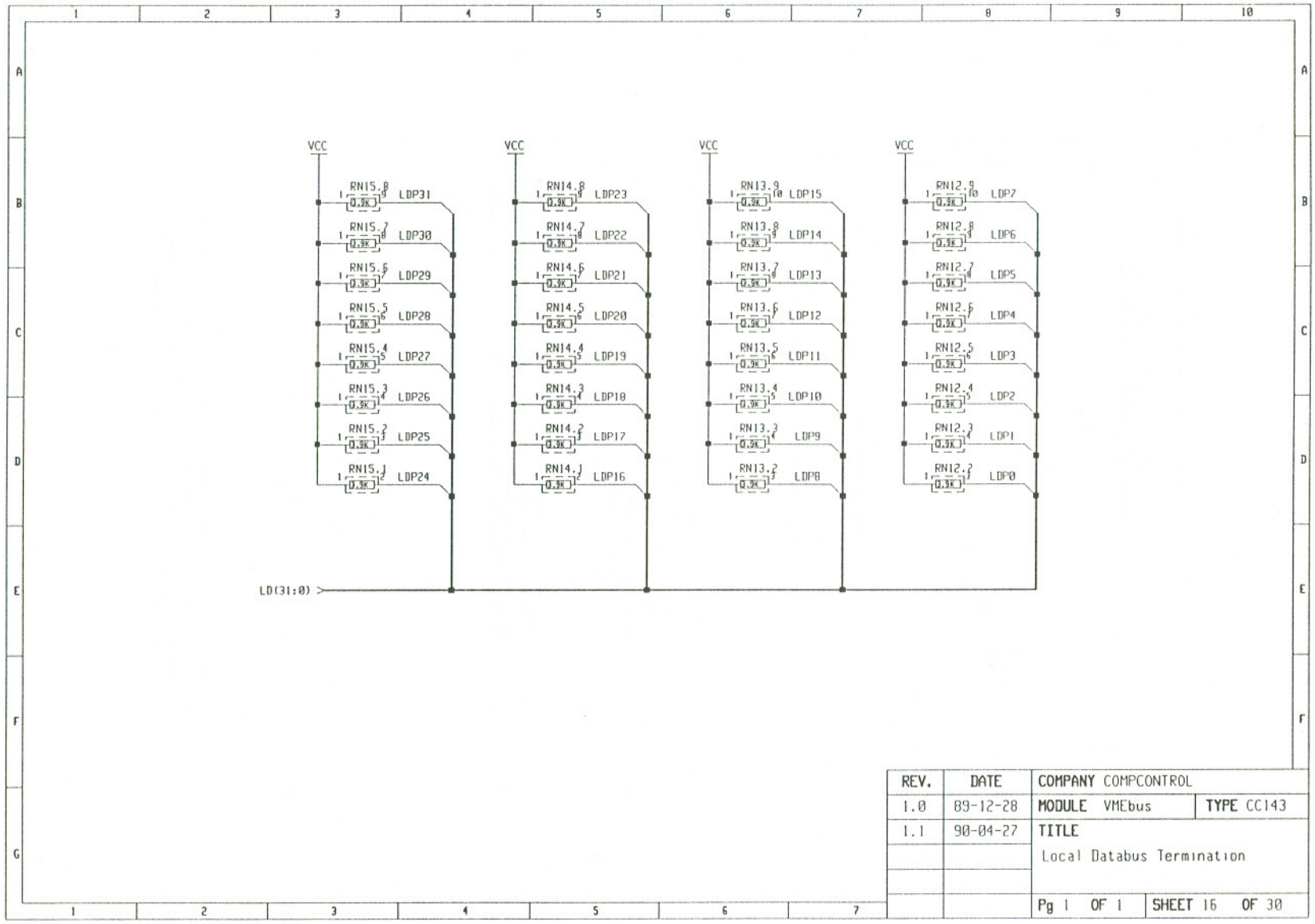

COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
1-Mbyte Video Memory
REV. DATE
1.0 89-12-28
1.1 90-04-27
Pg 1 OF 1
SHEET 11 OF 30
Byte3
Byte2
Byte1
Byte0
LD(31:24)
LD(23:16)
LD(15:8)
LD(7:0)
PXDD(7:0)
PXDC(7:0)
PXDB(7:0)
PXDA(7:0)
DSF0,RAS0~,WBWE0~
CAS(0:3)~,DTOE(0:3)~
MA(0:8)
SE0~,SC0


CMP4 DSF,RAS~,CAS(0:3)~,DT/OE(0:3)~,WB/WE~
U63
U59
U55
U51
U79
U75
U71
U67
TC524258Z-10
Video DRAM
Byte0
Byte1
Byte2
Byte3
LD(31:24)
PXDA(7:0)
LD(23:16)
PXDB(7:0)
LD(15:8)
PXDC(7:0)
LD(7:0)
PXDD(7:0)
DSF1,RAS1~,WBWE1~
CAS(0:3)~,DTOE(0:3)~
MA(8:0)
SE1~,SC1
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
1-Mbyte Video Memory
Pg 1 OF 1
SHEET 12 OF 30


CMP7|DSF,RAS~,CAS(0:3)~,DT/OE(0:3)~,WB/WE~
U64
U56
U80
U72
U60
U52
U76
U68
TC524258Z-10
Video DRAM
Byte0
Byte1
Byte2
Byte3
LD(31:24)
LD(23:16)
LD(15:8)
LD(7:0)
PXDA(7:0)
PXDB(7:0)
PXDC(7:0)
PXDD(7:0)
DSF0,RAS2~,WBWE0~
CAS(0:3)~,DTOE(0:3)~
MA(8:0)
SE2~,SC0
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
1-Mbyte Video Memory
Pg 1 OF 1
SHEET 13 OF 30


COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
1-Mbyte Video Memory
Pg 1 OF 1
SHEET 14 OF 30
REV. DATE
1.0 89-12-28
1.1 90-04-27
Byte3
Byte2
Byte1
Byte0
Video DRAM
TC524258Z-10
LD(31:24)
LD(23:16)
LD(15:8)
LD(7:0)
PXDA(7:0)
PXDB(7:0)
PXDC(7:0)
PXDD(7:0)
MA(8:0)
CAS(0:3)~,DTOE(0:3)~
RAS3~,WBWE1~
SE3~,SC1


SEL1 SEL0
G300 COL 0 0
G300 ROW 0 1
VME COL 1 0
VME ROW 1 1
MA(8:0)
MUA1 MUA2 MUA3 MUA4 MUA5 MUA6 MUA7 MUA8
CMPB|MUA(8:1)
GND
LD13 LD2 LA11
LD17 LD6 LA6 LA15
LD16 LD5 LA5 LA14
LD15 LD4 LA4 LA13
LD14 LD3 LA3 LA12
LD21 LD10 LA10 LA19
LD20 LD9 LA9 LA18
LD19 LD8 LA8 LA17
LD18 LD7 LA7 LA16
SEL0 >
SEL1 >
ENMUX >
LD(21:13) >
LD(10:2) >
LA(10:2) >
LA(19:11) >
REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
Address Multiplexers
Pg 1 OF 1
SHEET 15 OF 30



REV.	DATE	COMPANY COMPCONTROL	
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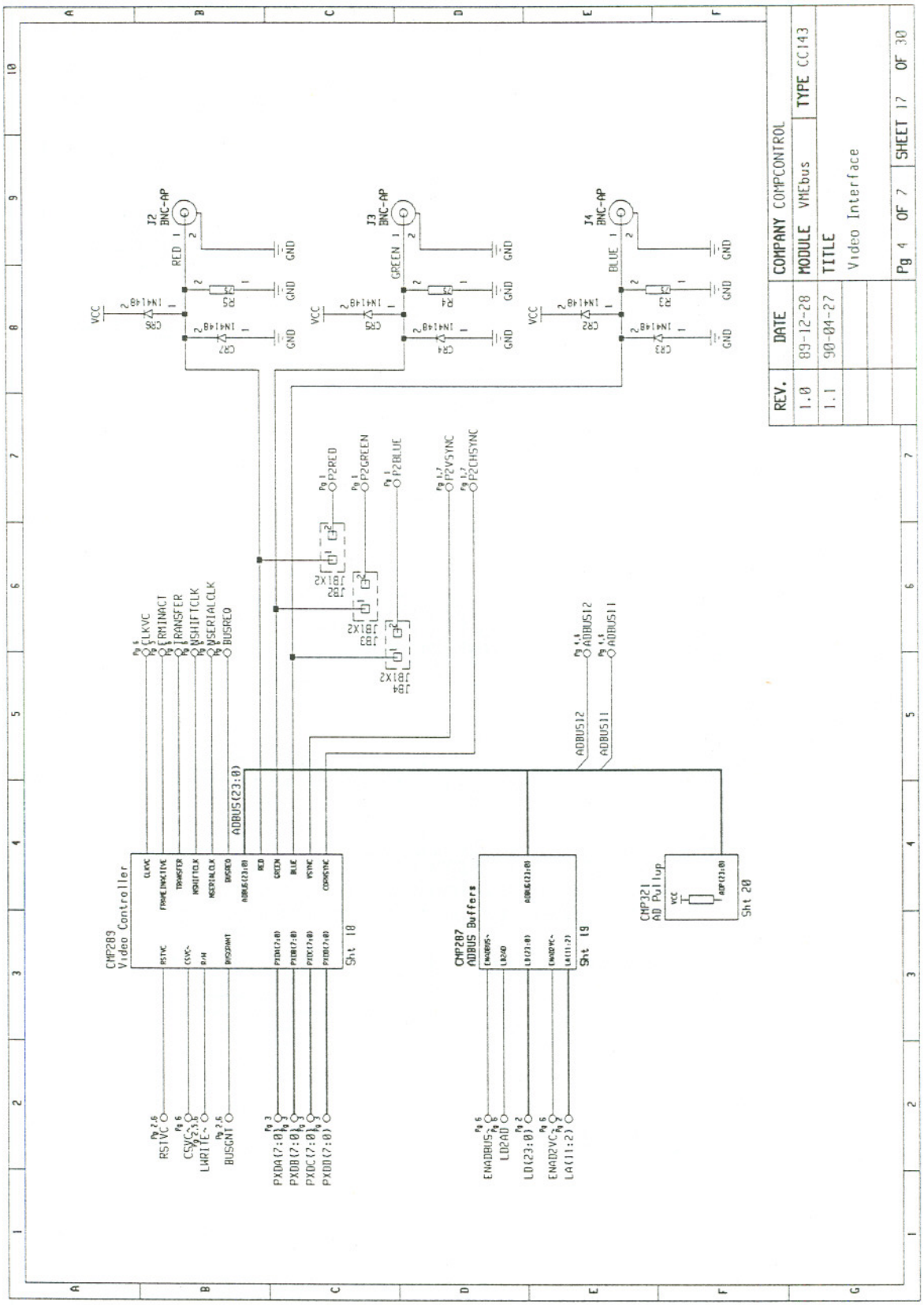
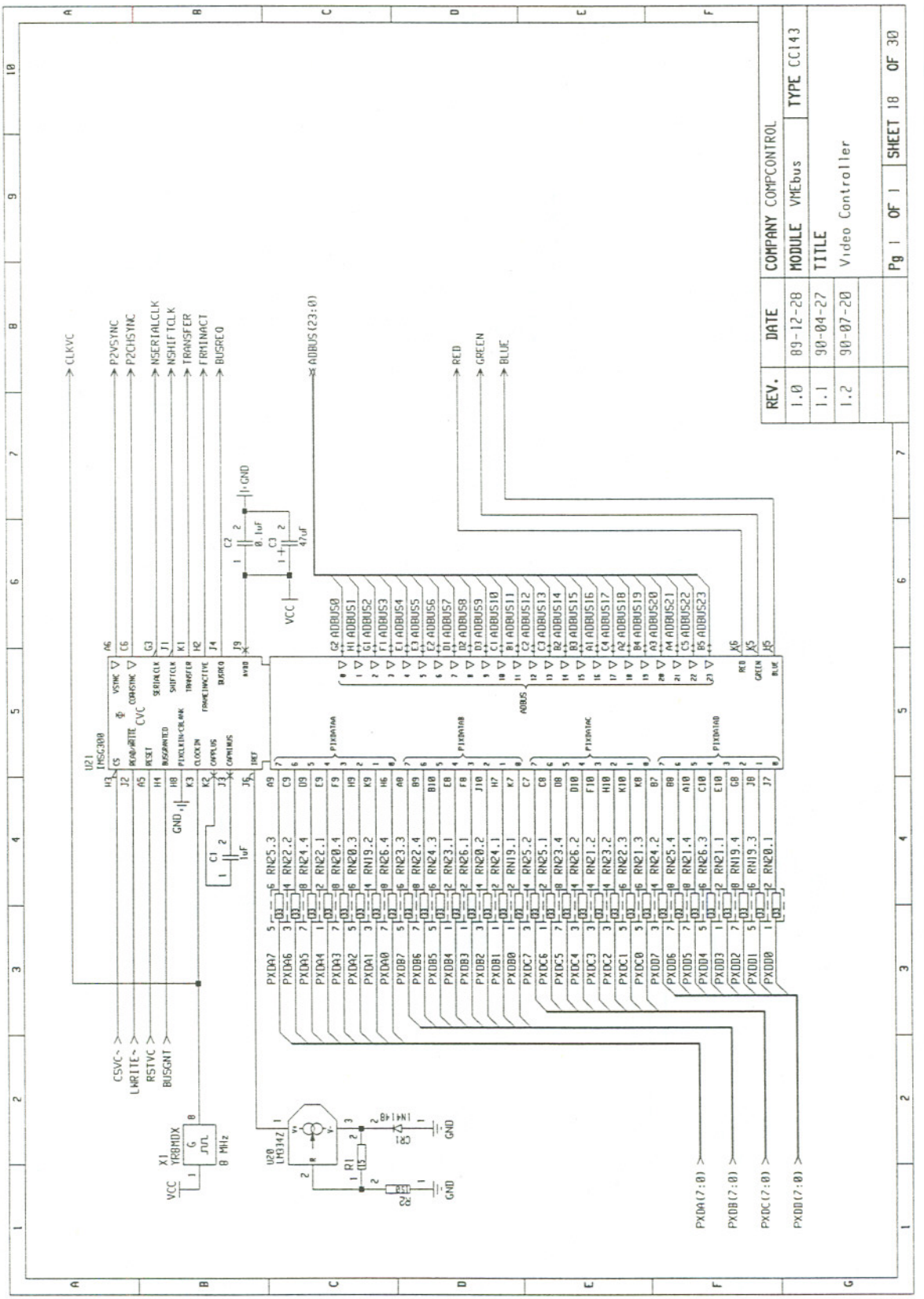
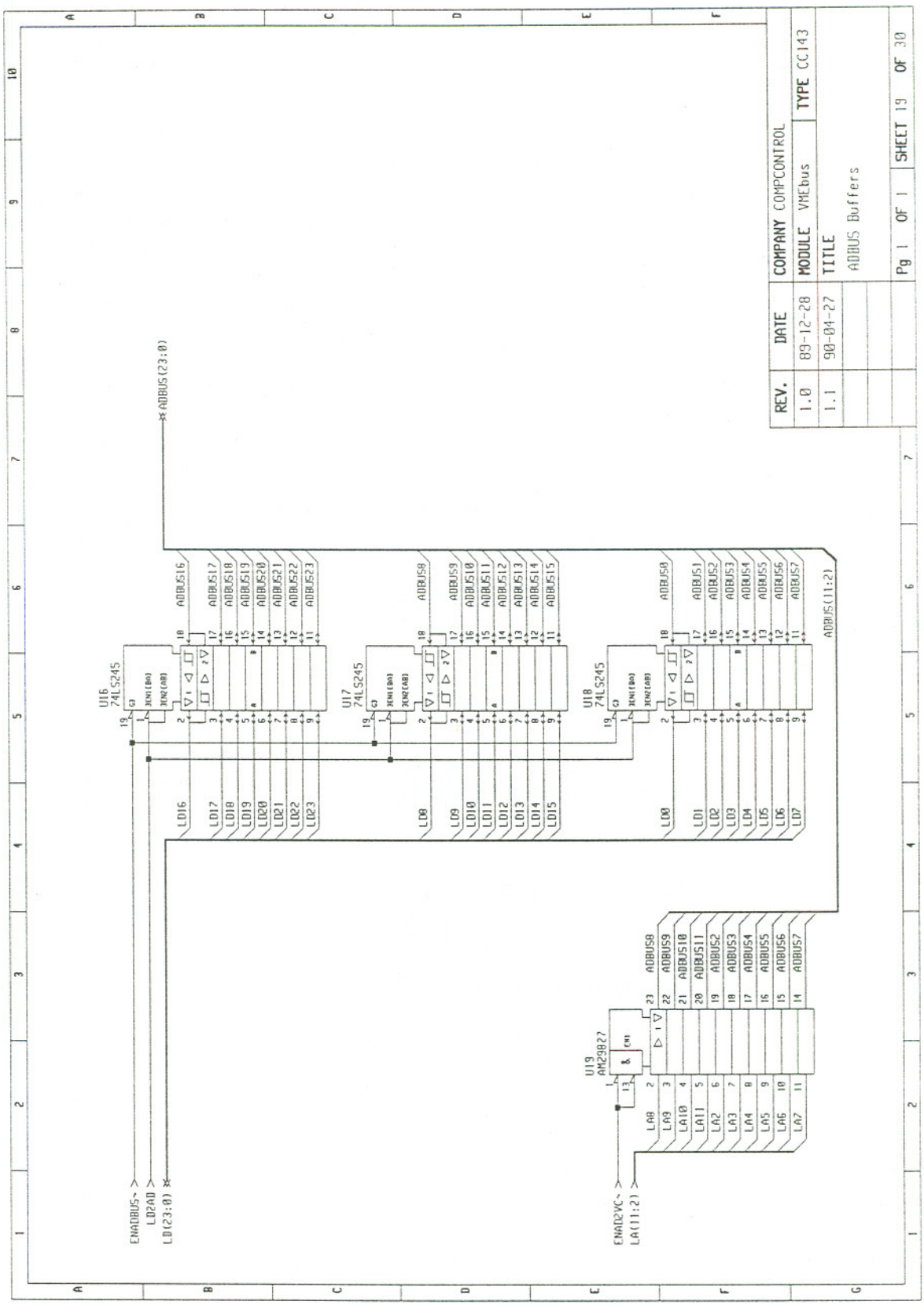
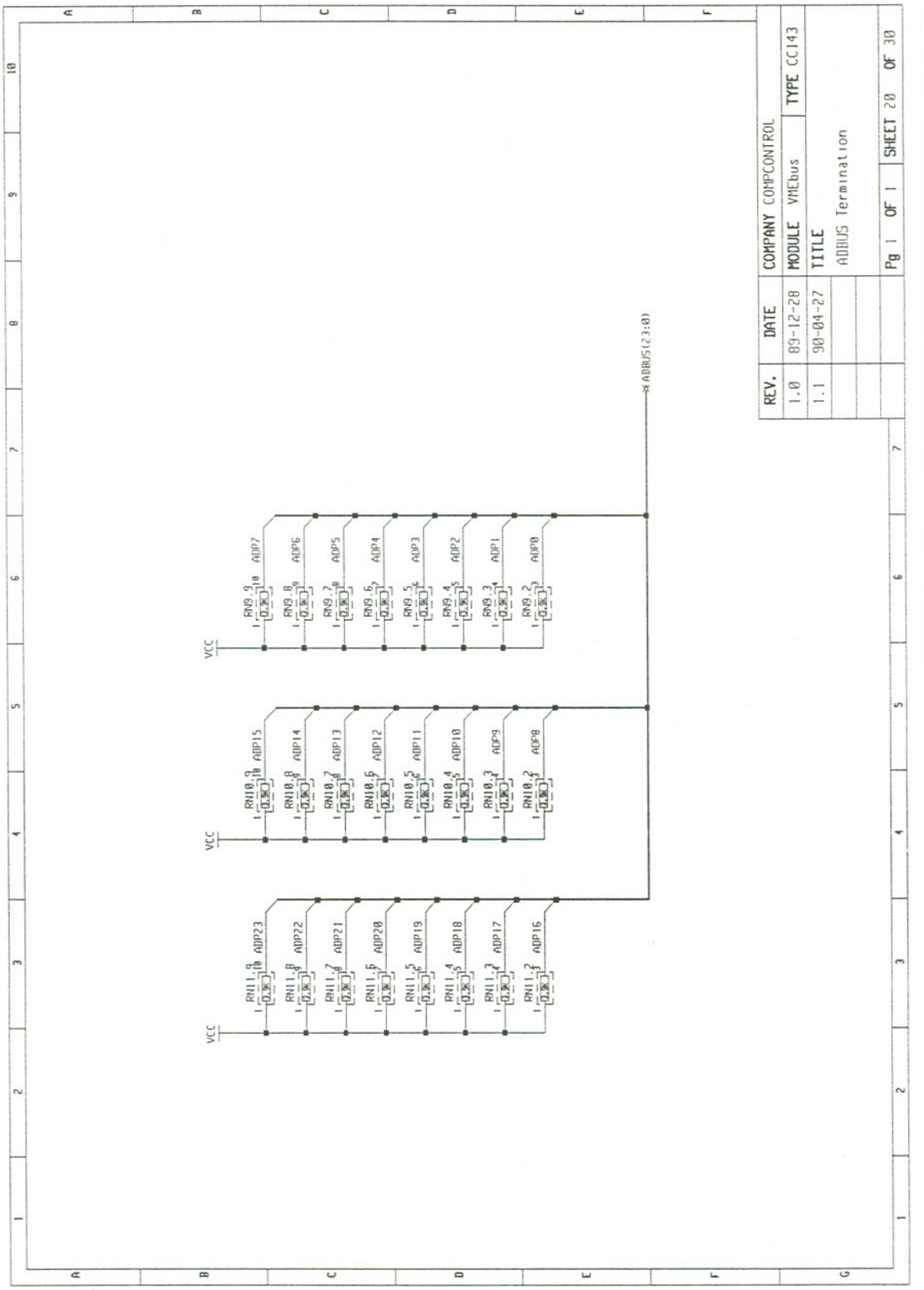
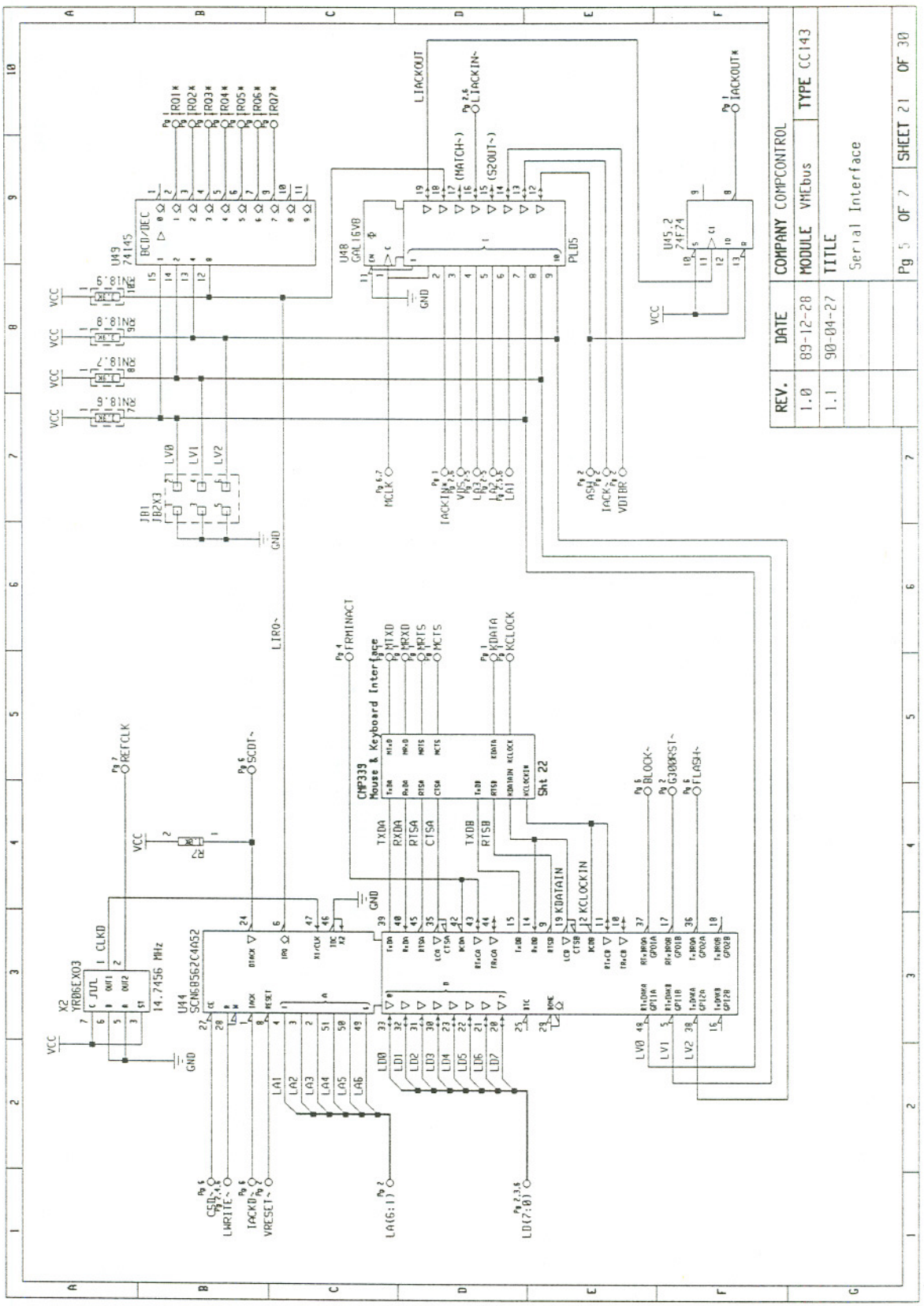
1.1	90-04-27	TITLE	
		Local Databus Termination	
		Pg 1 OF 1	SHEET 16 OF 30

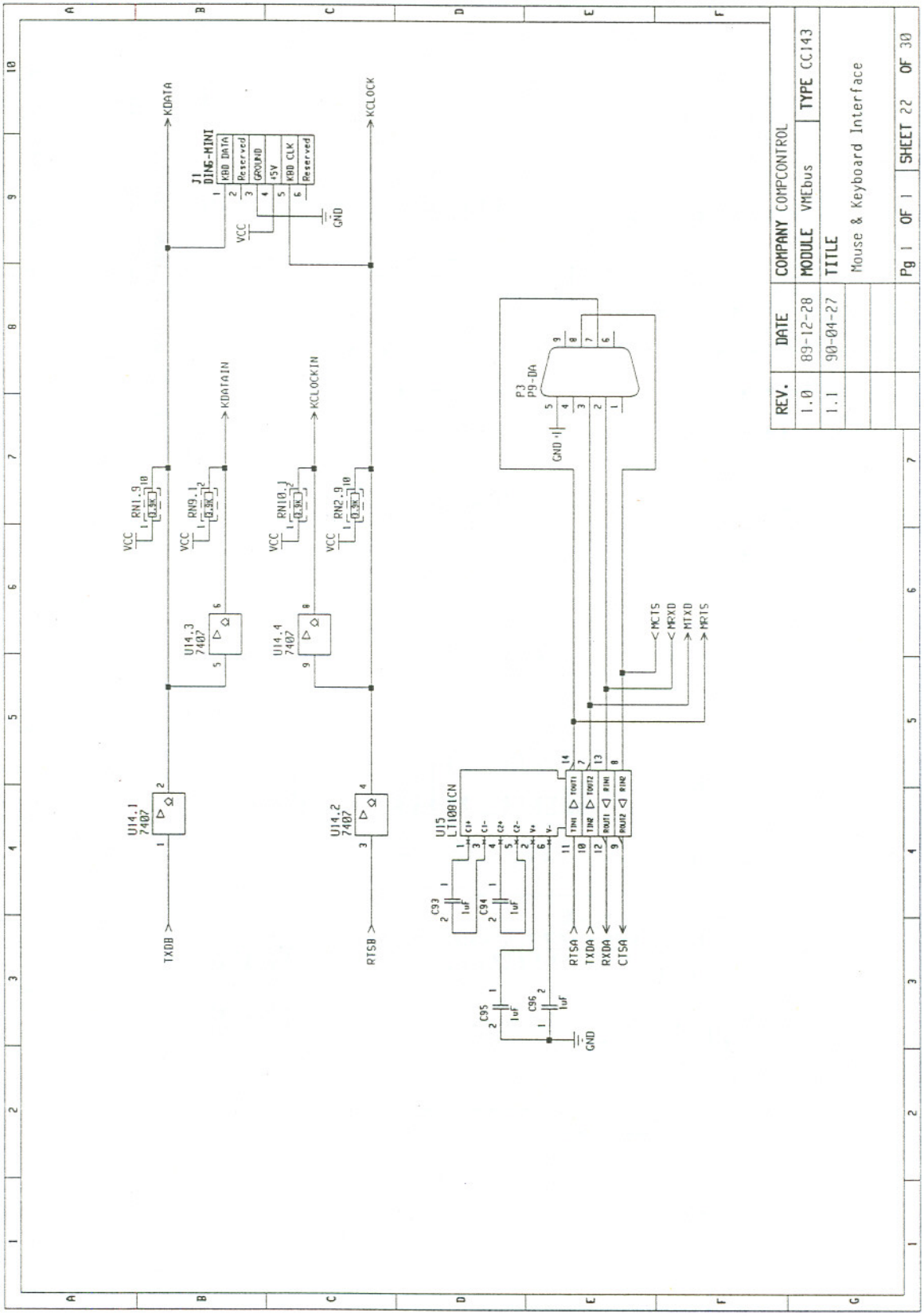

REV. | DATE | COMPANY COMPCONTROL
1.0 | 89-12-28 | MODULE VMEbus | TYPE CC143
1.1 | 90-04-27 | TITLE Video Interface
Pg 4 OF 7 | SHEET 17 OF 30
J2 BNC-AP
J3 BNC-AP
J4 BNC-AP
RED
GREEN
BLUE
GND
VCC
IN4148
R35
R34
R33
C86
C85
C82
C84
C83
P2RED
P2GREEN
P2BLUE
P2VSYNC
P2CHSYNC
ADBUS12
ADBUS11
ADBUS(23:0)
CLKVC
FRAMEINACTIVE
TRANSFER
MSHIFTCLK
MSERIALCLK
BUSREQ
CMP283
Video Controller
Sht 18
CMP287
ADBUS Buffers
Sht 19
CMP321
AD Pullup
Sht 20
RSTVC
CSVC
LWRITE
BUSGNT
PXDA(7:0)
PXDB(7:0)
PXDC(7:0)
PXDD(7:0)
ENADBUS
LD2AD
LD(23:0)
ENAD2VC
LA(11:2)

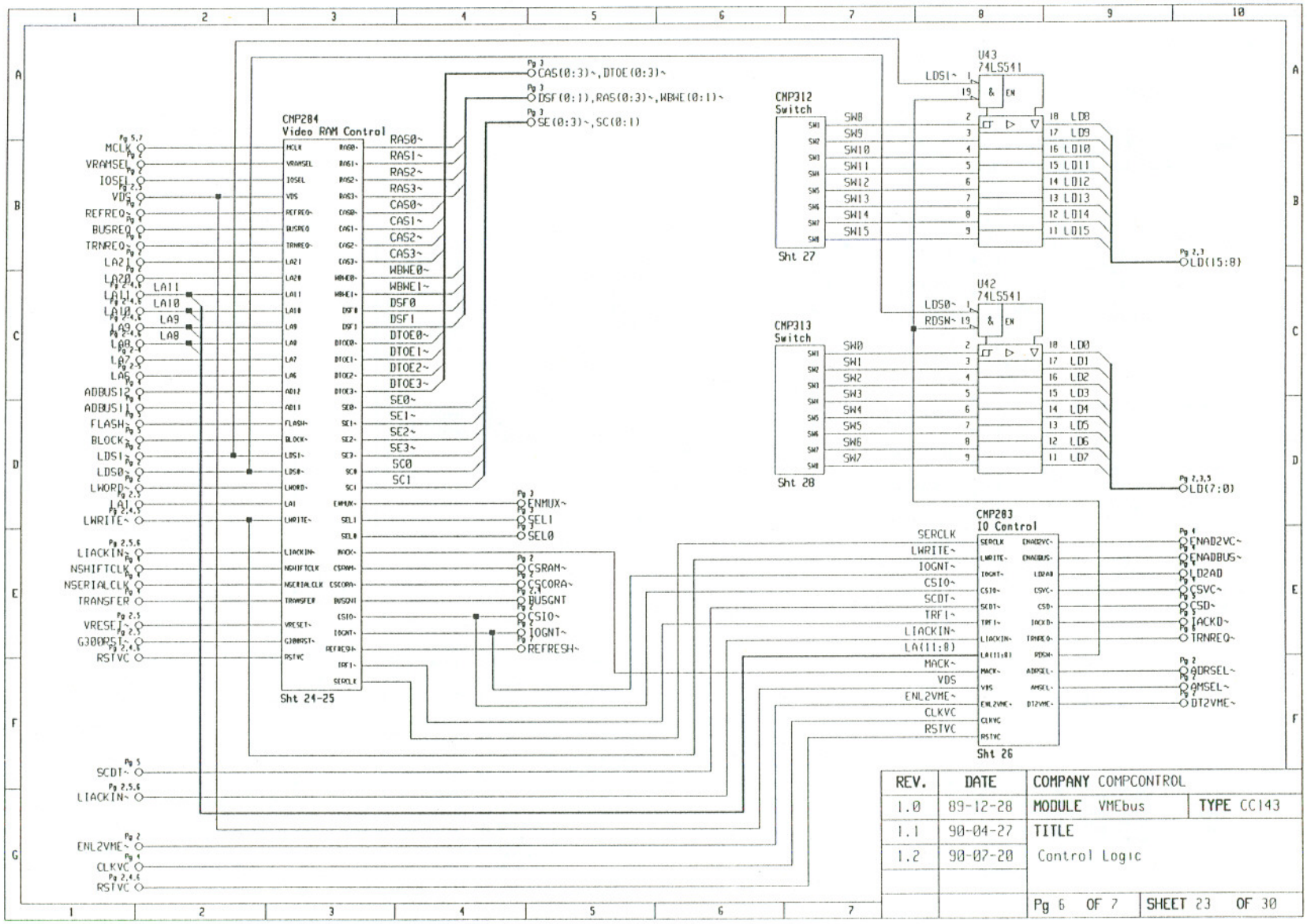

REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE
1.2 90-07-20 Video Controller
Pg 1 OF 1 SHEET 18 OF 30
CLKVC
P2VSYNC
P2CHSYNC
NSERIALCLK
NSHIFTCLK
TRANSFER
FRMINACT
BUSREQ
ADBUS(23:0)
RED
GREEN
BLUE
U21 IMSG300
U20 LM1342
X1 YRBMDX 8 MHz
C1 1uF
C2 0.1uF
C3 47uF
R1 0
R2
D1 1N4148
VCC
GND
CSVC~
LWRITE~
RSTVC
BUSGNT
PXDA(7:0)
PXDB(7:0)
PXDC(7:0)
PXDD(7:0)

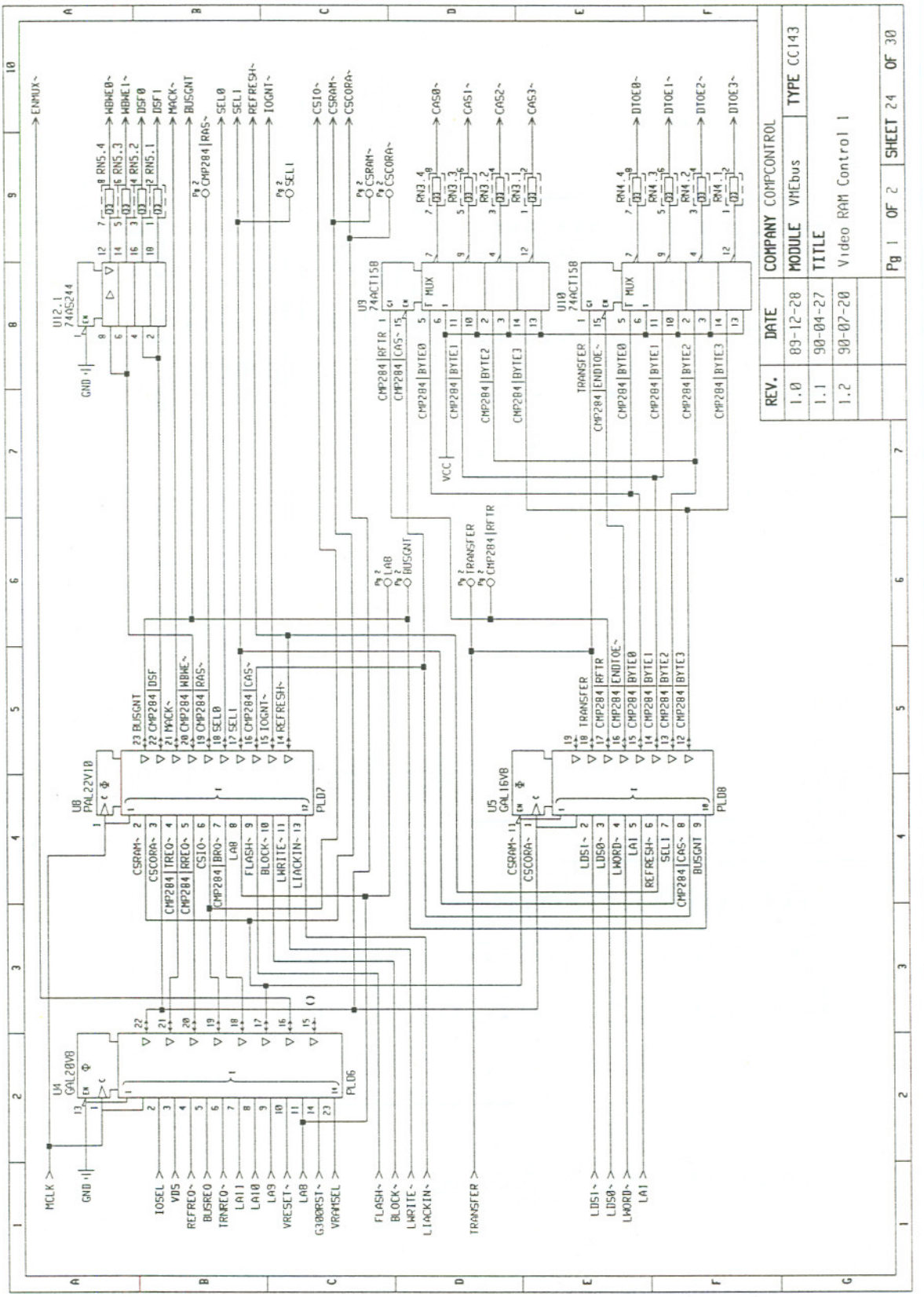

REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
ADBUS Buffers
Pg 1 OF 1
SHEET 19 OF 30
ADBUS(23:0)
ADBUS(11:2)
U16 74LS245
U17 74LS245
U18 74LS245
U19 AM29822
ENADBUS~
LD2AD
LD(23:0)
ENAD2VC~
LA(11:2)

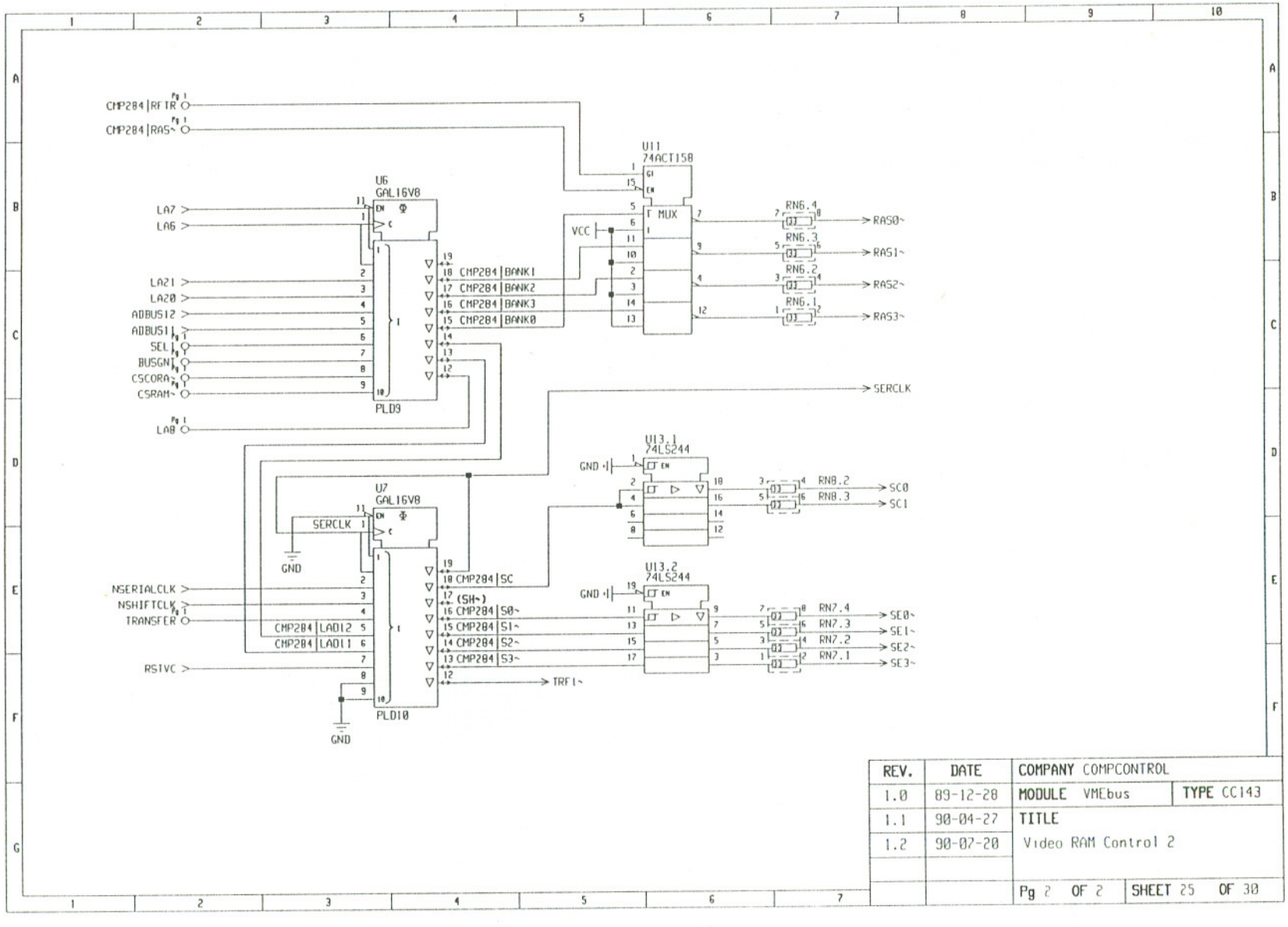

ADBUS(23:0)
VCC
RN9.9 10 ADP7
RN9.8 9 ADP6
RN9.7 8 ADP5
RN9.6 7 ADP4
RN9.5 6 ADP3
RN9.4 5 ADP2
RN9.3 4 ADP1
RN9.2 3 ADP0
RN10.9 10 ADP15
RN10.8 9 ADP14
RN10.7 8 ADP13
RN10.6 7 ADP12
RN10.5 6 ADP11
RN10.4 5 ADP10
RN10.3 4 ADP9
RN10.2 3 ADP8
RN11.9 10 ADP23
RN11.8 9 ADP22
RN11.7 8 ADP21
RN11.6 7 ADP20
RN11.5 6 ADP19
RN11.4 5 ADP18
RN11.3 4 ADP17
RN11.2 3 ADP16
REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
ADBUS Termination
Pg 1 OF 1
SHEET 20 OF 30


REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE Serial Interface
Pg 5 OF 7 SHEET 21 OF 30
CMF339 Mouse & Keyboard Interface
Sht 22
U44 SCN68562C4A52
U49 74145
U48 GAL16V8
U45.2 74F24
X2 YRB6EX03 14.7456 MHz
JB1 JB2X3
R1 R2 R3 R4 R5 R6 R7 R8
VCC
GND
REFCLK
SCDT~
LIRQ~
TXDA RXDA RTSA CTSA TXDB RTSB
KDATAIN KCLOCKIN
BLOCK~
G300RST~
FLASH~
LA1 LA2 LA3 LA4 LA5 LA6
LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7
LV0 LV1 LV2
CSD~ LWRITE~ IACKD VRESET~
LA(6:1) LD(7:0)
LIACKOUT IACKIN~ IACKOUT
(MATCH-) (S2OUT-)
MCLK AS4 IACK VDTBR
MTXD MRXD MRTS MCTS
KDATA KCLOCK
IRM1NACT

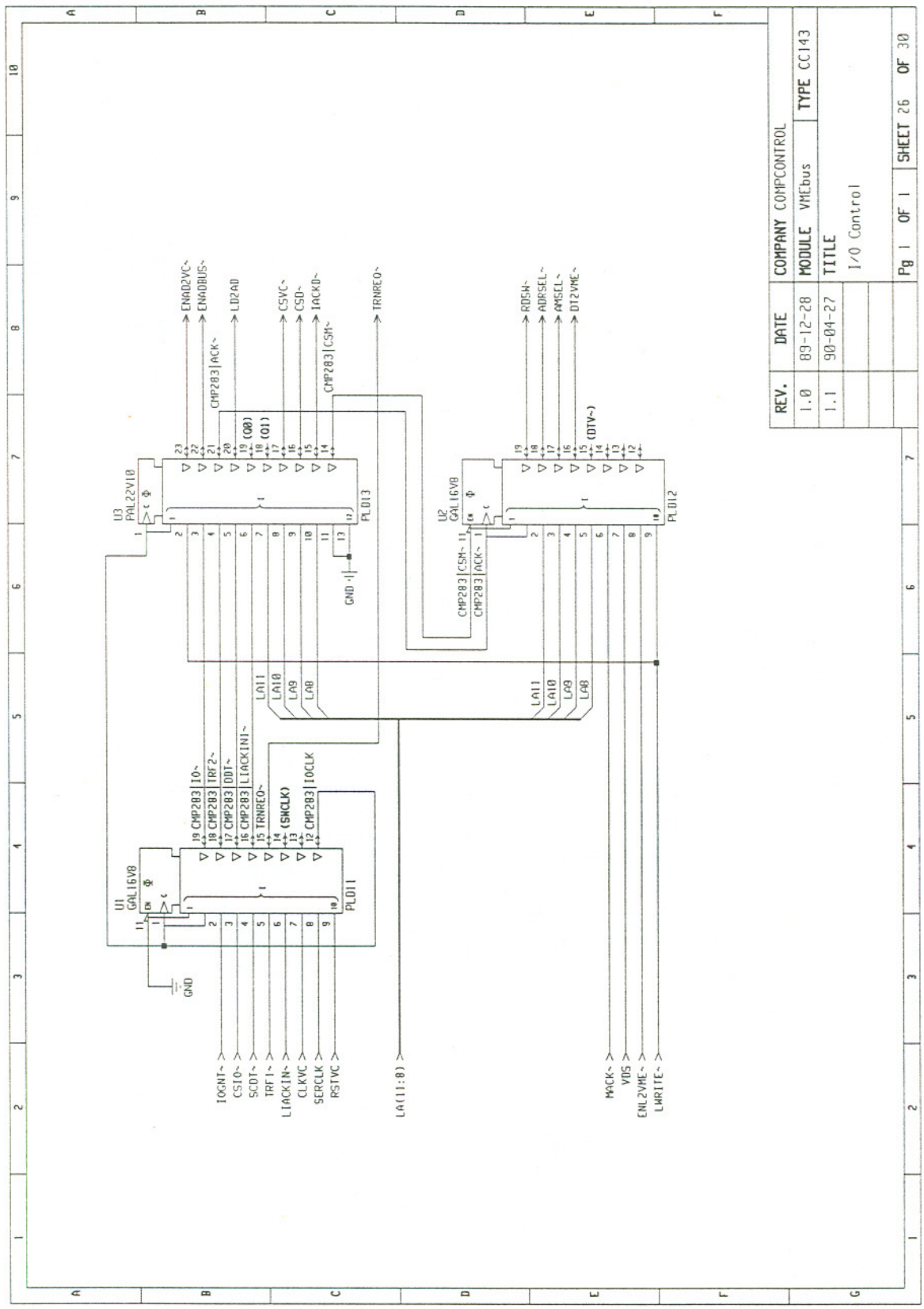

KDATA
KCLOCK
J1
DIN6-MINI
KBD DATA
Reserved
GROUND
+5V
KBD CLK
Reserved
VCC
GND
KDATAIN
KCLOCKIN
RN1,9
RN9,1
RN10,1
RN2,9
10K
U14,1
U14,2
U14,3
U14,4
7407
TXDB
RTSB
P3
P9-DA
GND
MCTS
MRXD
MTXD
MRTS
U15
LT1081CN
C93
C94
C95
C96
1uF
RTSA
TXDA
RXDA
CTSA
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
Mouse & Keyboard Interface
Pg 1 OF 1
SHEET 22 OF 30

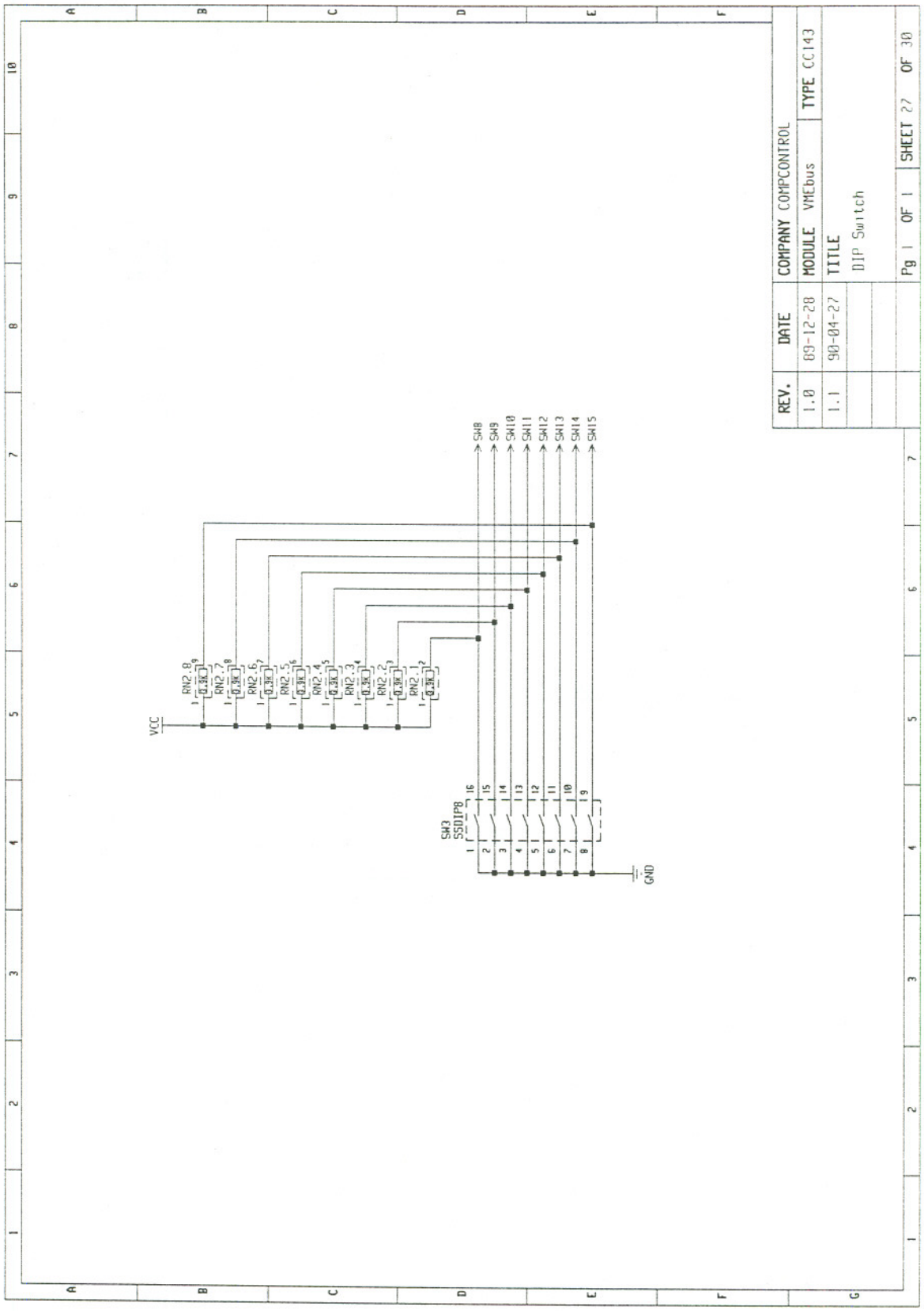

CMP284
Video RAM Control
Sht 24-25
CMP312
Switch
Sht 27
CMP313
Switch
Sht 28
U43
74LS541
U42
74LS541
CMP283
IO Control
Sht 26
MCLK
VRAMSEL
IOSEL
VDS
REFREQ~
BUSREQ
TRNREQ~
LA21
LA20
LA11
LA10
LA9
LA8
LA7
LA6
ADBUS12
ADBUS11
FLASH~
BLOCK~
LDS1~
LDS0~
LWORD~
LA1
LWRITE~
LIACKIN~
NSHIFTCLK
NSERIALCLK
TRANSFER
VRESET~
G300RST~
RSTVC
SCDT~
ENL2VME~
CLKVC
RSTVC
RAS0~
RAS1~
RAS2~
RAS3~
CAS0~
CAS1~
CAS2~
CAS3~
WBWE0~
WBWE1~
DSF0
DSF1
DTOE0~
DTOE1~
DTOE2~
DTOE3~
SE0~
SE1~
SE2~
SE3~
SC0
SC1
CAS(0:3)~,DTOE(0:3)~
DSF(0:1),RAS(0:3)~,WBWE(0:1)~
SE(0:3)~,SC(0:1)
ENMUX~
SEL1
SEL0
CSRAM~
CSCORA~
BUSGNT
CSIO~
IOGNT~
REFRESH~
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
LD8
LD9
LD10
LD11
LD12
LD13
LD14
LD15
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD(15:8)
LD(7:0)
SERCLK
LWRITE~
IOGNT~
CSIO~
SCDT~
TRF1~
LIACKIN~
LA(11:8)
MACK~
VDS
ENL2VME~
CLKVC
RSTVC
ENAD2VC~
ENADBUS~
LD2AD
CSVC~
CSD~
IACKD~
TRNREQ~
ADRSEL~
AMSEL~
DT2VME~
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
1.2
90-07-20
Control Logic
Pg 6 OF 7
SHEET 23 OF 30

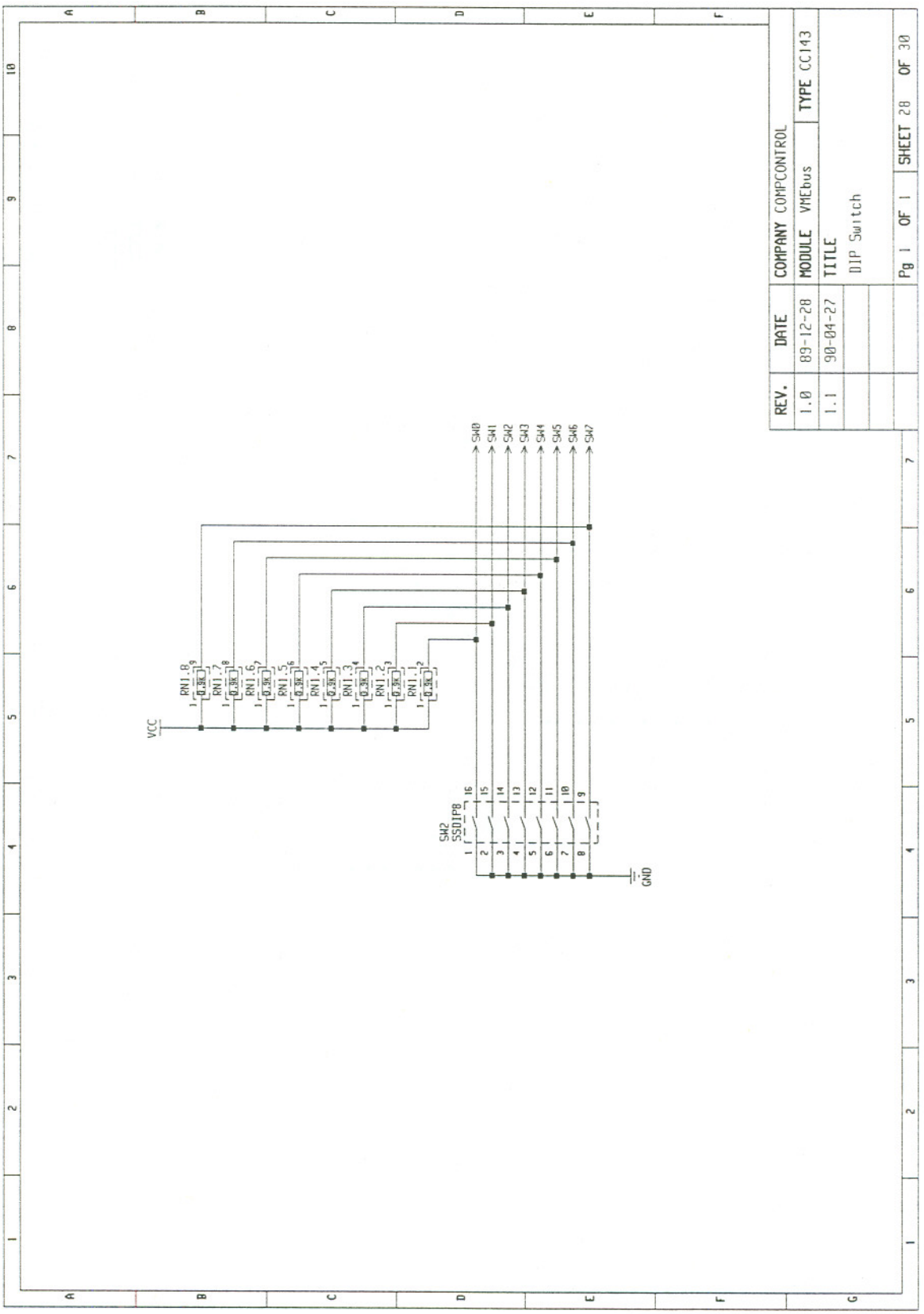

COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
Video RAM Control 1
Pg 1 OF 2
SHEET 24 OF 30
REV. DATE
1.0 89-12-28
1.1 90-04-27
1.2 90-07-20
U8 PAL22V10
U4 GAL20V8
U5 GAL16V8
U9 74ACT158
U10 74ACT158
U12.1 74AS244
MCLK
GND
IOSEL
VDS
REFREQ~
BUSREQ
TRNREQ~
LA11
LA10
LA9
VRESET~
LA8
G300RST~
VRAMSEL
FLASH~
BLOCK~
LWRITE~
LIACKIN~
TRANSFER
LDS1~
LDS0~
LWORD~
LA1
ENMUX~
WBWE0~
WBWE1~
DSF0
DSF1
MACK~
BUSGNT
SEL0
SEL1
REFRESH~
IOGNT~
CS10~
CSRAM~
CSCORA~
CAS0~
CAS1~
CAS2~
CAS3~
DTOE0~
DTOE1~
DTOE2~
DTOE3~
RN3.4
RN3.3
RN3.2
RN3.1
RN4.4
RN4.3
RN4.2
RN4.1
RN5.4
RN5.3
RN5.2
RN5.1
VCC
PLD6
PLD7
PLD8

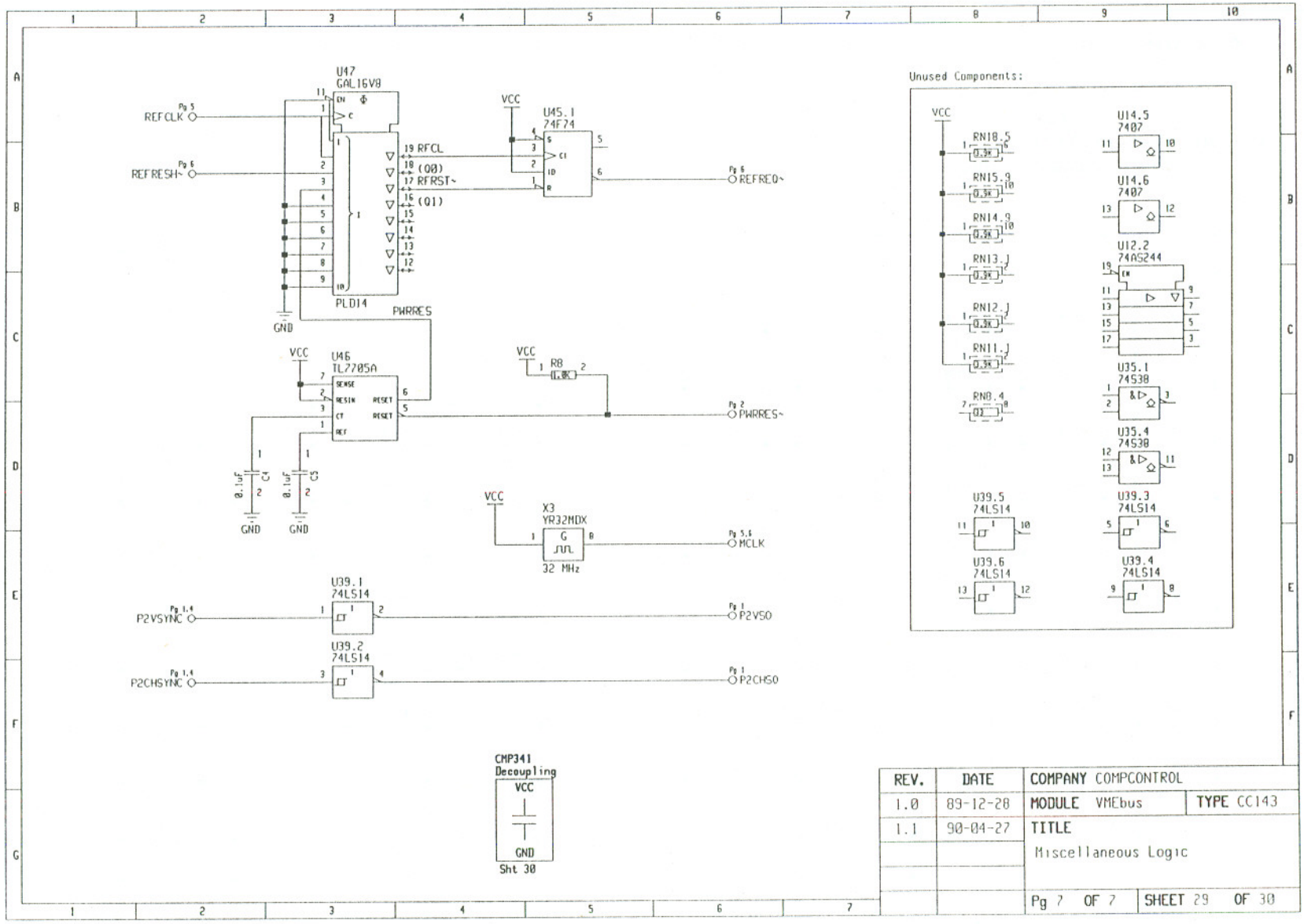


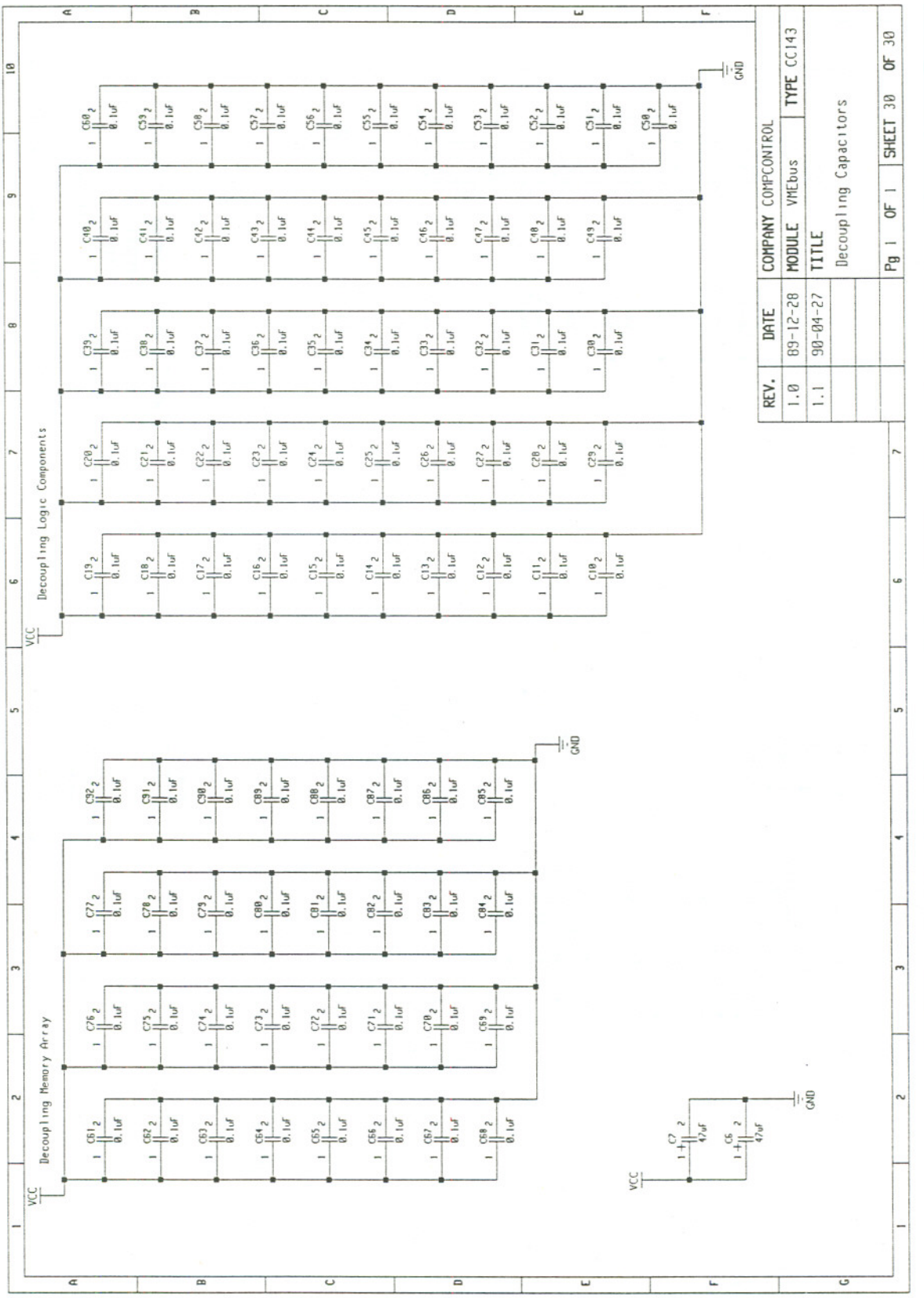
REV.	DATE	COMPANY COMPCONTROL	
1.0	89-12-28	MODULE VMEbus	TYPE CC143
1.1	90-04-27	TITLE	
1.2	90-07-20	Video RAM Control 2	
		Pg 2 OF 2	SHEET 25 OF 30


REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE I/O Control
Pg 1 OF 1
SHEET 26 OF 30
U1 GAL16V8
U2 GAL16V8
U3 PAL22V10
PLD11
PLD12
PLD13
GND
ENAD2VC~
ENADBUS~
LD2AD
CSVC~
CSD~
IACKD~
TRNREQ~
RDSN~
ADRSEL~
AMSEL~
DT2VME~
CMP283|ACK~
CMP283|CSM~
CMP283|IO~
CMP283|TRF2~
CMP283|DDT~
CMP283|LIACKIN1~
CMP283|IOCLK
(SWCLK)
LA11
LA10
LA9
LA8
IOGNT~
CSIO~
SCDT~
TRFI~
LIACKIN~
CLKVC
SERCLK
RSTVC
LA(11:8)
MACK~
VDS
ENL2VME~
LWRITE~


REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE DIP Switch
Pg 1 OF 1 SHEET 27 OF 30
VCC
RN2.8 RN2.7 RN2.6 RN2.5 RN2.4 RN2.3 RN2.2 RN2.1
0.3K
SW3 S5DIP8
SW8 SW9 SW10 SW11 SW12 SW13 SW14 SW15
GND

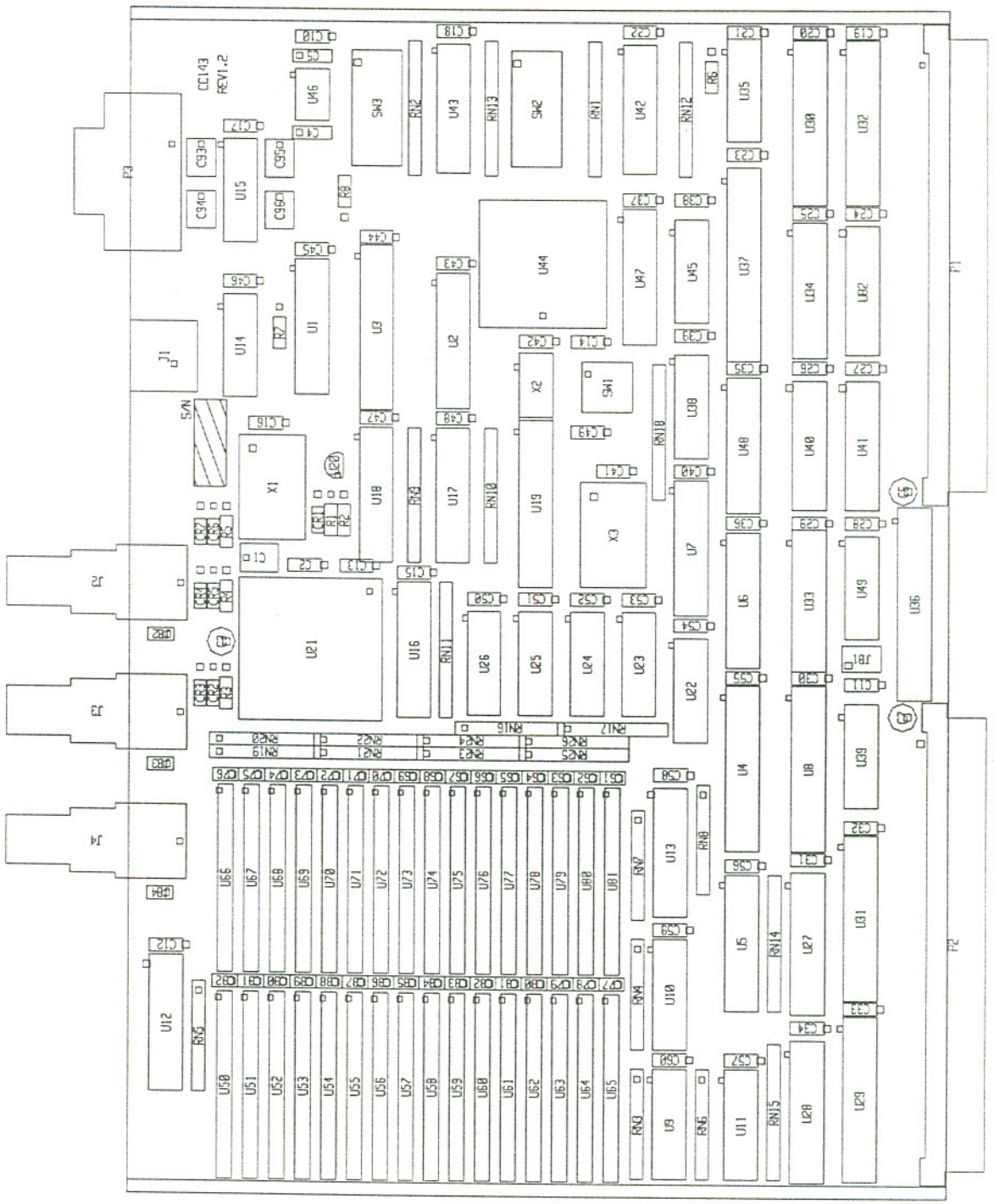

REV. DATE
1.0 89-12-28
1.1 90-04-27
COMPANY COMPCONTROL
MODULE VMEbus
TYPE CC143
TITLE
DIP Switch
Pg 1 OF 1
SHEET 28 OF 30
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
RN1.8
RN1.7
RN1.6
RN1.5
RN1.4
RN1.3
RN1.2
RN1.1
0.5K
VCC
SW2
SSDIP8
GND


U47
GAL16V8
REFCLK
REFRESH~
PLD14
PWRRES
U45.1
74F74
RFCL
(Q0)
RFRST~
(Q1)
REFREQ~
U46
TL7705A
SENSE
RESIN
CT
REF
RESET
RESET
RB
PWRRES~
C4
C5
0.1uF
GND
X3
YR32MDX
32 MHz
MCLK
U39.1
74LS14
P2VSYNC
P2VS0
U39.2
74LS14
P2CHSYNC
P2CHS0
VCC
Unused Components:
RN18.5
RN15.9
RN14.9
RN13.J
RN12.J
RN11.J
RN8.4
U14.5
7407
U14.6
7407
U12.2
74AS244
U35.1
74S38
U35.4
74S38
U39.5
74LS14
U39.3
74LS14
U39.6
74LS14
U39.4
74LS14
CMP341
Decoupling
Sht 30
REV.
DATE
COMPANY COMPCONTROL
1.0
89-12-28
MODULE VMEbus
TYPE CC143
1.1
90-04-27
TITLE
Miscellaneous Logic
Pg 7 OF 7
SHEET 29 OF 30


Decoupling Logic Components
Decoupling Memory Array
VCC
GND
REV. DATE COMPANY COMPCONTROL
1.0 89-12-28 MODULE VMEbus TYPE CC143
1.1 90-04-27 TITLE Decoupling Capacitors
Pg 1 OF 1 SHEET 30 OF 30

Appendix C Component Layout

Figure C-1 Component Layout CC143



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Appendix D List of Components

Integrated Circuits (TTL)

U9-U11	74ACT158	Quad 2-input multiplexer
U12	74AS244	Octal bus driver ninv 3-state
U13	74LS244	Octal bus driver ninv 3-state
U14	7407	Hex buffer driver o.c.
U16-U18	74LS245	Octal transceiver ninv 3-state
U19	AM29827	10-bit buffer line driver ninv 3-st
U22-U26	74AS153	Dual 4-input multiplexer
U27,U28	74F245	Octal transceiver ninv 3-state
U29-U32	74F543	Octal registered transceiver
U35	74S38	Quad 2-input NAND o.c.
U38	74S85	4-bit magnitude comparator
U39	74LS14	Hex inverter
U40,U41,U82	74ALS573	Octal D-type transparent latch 3-st
U42,U43	74LS541	Octal buffer, line driver 3-state
U45	74F74	Dual D-type flip-flop
U49	74145	BCD-to-decimal decoder/driver

Integrated Circuits (PLD)

U1	143-001-1	PLD11 GAL16V8-20
U2	143-002-0	PLD12 GAL16V8-20
U3	143-003-1	PLD13PAL22V10-20
U4	143-004-2	PLD6 GAL20V8-20
U5	143-005-0	PLD8GAL16V8-20
U6	143<x>006-1	PLD9<x> GAL16V8-20
U7	143-007-1	PLD10 GAL16V8-20
U8	143-008-1	PLD7 PAL22V10-20
U33	143-033-1	PLD4 PLS153
U34	143-034-1	PLD3 GAL16V8-20
U36	143<x>036-1	PLD1<x> EPM5032DC-2
U37	143-037-1	PLD2 EPM5032DC-2
U47	143-047-1	PLD14 GAL16V8-20
U48	143-048-1	PLD5 GAL16V8-20

Memory Devices

U50-U81	TC524256Z-10	256Kx4 multi-port Dram 100ns
	TC524257Z-10	+Raster operations
	TC524258Z-10	+Special Write Functions

Integrated Circuits (Miscellaneous)

X1	YR8MDX	5 or 8 MHz clock generator
X2	YR06EXO3	14.7456 MHz clock generator
X3	YR32MDX	32 MHz clock generator
U15	LT1081CN	Dual line driver/receiver
U20	LM334Z	Precision current reference
U21	IMSG300	Color video controller 84-pin PGA socket
U44	SCN68562C4A52	Dual universal serial comm. contr. 52-pin PLCC socket
U46	TL7705A	Supply voltage supervisor

Capacitors

C1,C93-C96	WIMA-MKS2-1UF	1 μF/25V
C3,C6,C7	ELCO2222035479	non-solid alu elco 47 μF/16V
C4,C5		0.1 μF (0.2")
C2,C10-C60	AVXMD015C104K	0.1 μF (0.3")
C61-C92	VP32BY104MAD006	0.1 μF (0.1")

Resistors

R1	RSFR25159	Standard film 15 ohm 5%
R2	RSFR25151	Standard film 150 ohm 5%
R3-R5	RSFR25759	Standard film 75 ohm 5%
R6-R8	RSFR25102	Standard film 1k ohm 5%

Resistor Networks

RN1,RN2	RNS9BUS392	4610X-101 3k9 pull-up
RN9-RN15,RN18	RNS9BUS392	4610X-101 3k9 pull-up
RN3-RN8	RNS4ISO330	4608X-102 33 ohm series
RN16,RN17	RNS4ISO330	4608X-102 33 ohm series
RN19-RN26	RNS4ISO330	4608X-102 33 ohm series

Connectors/Jumpers

P1-P2	P96ABC-EA	96-pin IEC 603 male connector
P3	P9-DA	9-pin D-type male connector
J1	DIN6-MINI	6-pin mini DIN connector
J2-J4	BNC-AP	BNC connector
JB1	JB2X3	2x3-pin jumper block
JB2-JB4	JB1X2	1x2-pin jumper block

Diodes

CR1-CR7	1N4148	Diode

Switches

SW1	SSDRD16C	Rotary hexadecimal dip switch
SW2,SW3	SSDIP8	16-pin dip switch

Note: Some parts may have been replaced by their equivalent types.

Appendix E Connector Assignments

This Appendix identifies the VMEbus connectors P1, P2, the I/O connectors P3, and J1.

VMEbus P1

Table E-1 P1 Pin Assignments

P1 Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	(SYSCLK)	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12V)	(+5V STDBY)	(+12V)
32	+5V	+5V	+5V

NOTE: Signal mnemonics shown in parenthesis are not used by the CC143 module.

VMEbus P2

Table E-2 P2 Pin Assignments

P2 Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	+5 VOLT	+5 VOLT	+5 VOLT
2	GND	GND	GND
3		(RESERVED)	
4		A24	
5		A25	
6	MRXD	A26	
7	MRTS	A27	
8	MTXD	A28	
9	MCTS	A29	
10		A30	
11		A31	
12	GND	GND	GND
13	+5 VOLT	+5 VOLT	+5 VOLT
14	GND	D16	GND
15		D17	
16	KDATA	D18	GND
17	KCLOCK	D19	GND
18		D20	
19		D21	
20		D22	
21		D23	
22	GND	GND	GND
23	P2VSYNC	D24	P2VSO
24	GND	D25	GND
25	P2CHSYNC	D26	P2CHSO
26	GND	D27	GND
27	P2BLUE	D28	GND
28	GND	D29	GND
29	P2GREEN	D30	GND
30	GND	D31	GND
31	P2RED	GND	GND
32	GND	+5 VOLT	GND

NOTE: Signal mnemonics shown in parenthesis are not used by the CC143 module.

Serial Port P3

P3 Pin Assignments

P3 Pin Number	CC143 Signal Mnemonic
1	n.c.
2	MRXD
3	MTXD
4	n.c.
5	GND
6	n.c.
7	MRTS
8	MCTS
9	n.c.

Keyboard Interface Connector J1

Table E-3 J1 Pin Assignments

J1 Pin Number	CC143 Signal Mnemonic
1	KBD Data
2	reserved
3	GND
4	+5 VOLT
5	KBD Clock
6	reserved

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Appendix F Short I/O Memory Map

name	start	end	size
G300			
Color Lookup Table	x000	x3FF	24
Byte Counter	x400	x403	24
HalfSync	x484	x487	24
BackPorch	x488	x48B	24
Display	x48C	x48F	24
ShortDisplay	x490	x493	24
BroadPulse	x494	x497	24
Vsync	x498	x49B	24
VBlank	x49C	x49F	24
VDisplay	x4A0	x4A3	24
LineTime	x4A4	x4A7	24
LineStart	x4A8	x4AB	24
MemInit	x4AC	x4AF	24
TransferDelay	x4B0	x4B4	24
Mask Register	x500	x503	24
Control Register	x580	x583	24
Top of Screen Register	x600	x603	24
Boot Location	x680	x683	24
Raster Operation Code Registers			
Raster Operation ZERO	x800	x803	32
Raster Operation AND1	x804	x807	32
Raster Operation AND2	x808	x80B	32
Raster Operation INHIBIT	x80C	x80F	32
Raster Operation AND3	x810	x813	32
Raster Operation THRU	x814	x817	32
Raster Operation EOR	x818	x81B	32
Raster Operation OR1	x81C	x81F	32
Raster Operation NOR	x820	x823	32
Raster Operation ENOR	x824	x827	32
Raster Operation INV1	x828	x82B	32
Raster Operation OR2	x82C	x82F	32
Raster Operation INV2	x830	x833	32
Raster Operation OR3	x834	x837	32
Raster Operation NAND	x838	x83B	32
Raster Operation ONE	x83C	x83F	32
Color Register			
Color Register	x900	x903	32
Address Decoder Registers			
Address Register A31-A28	xA01		4
Address Register A27-A24	xA03		4
Address Register A23-A20	xA05		4
Version Register	xA07		4
AM-code Register 1	xB01		4
AM-code Register 2	xB03		4
DIP Switch Registers			
SW3 Register	xC00		8
SW2 Register	xC01		8
Serial Interface (DUSCC)			
DUSCC Registers	xD01	xD7F	8 (see next page)

Table F-1 DUSCC Register Address Map

Address Channel A	Address Channel B	Acronym	Register Name
xD01	xD41	CMR1	Channel Mode Register 1
xD03	xD43	CMR2	Channel Mode Register 2
xD05	xD45	S1R	SYN 1/Secondary Address 1 Register
xD07	xD47	S2R	SYN 2/Secondary Address 2 Register
xD09	xD49	TPR	Transmitter Parameter Register
xD0B	xD4B	TTR	Transmitter Timing Register
xD0D	xD4D	RPR	Receiver Parameter Register
xD0F	xD4F	RTR	Receiver Timing Register
xD11	xD51	CTPRH	Counter/Timer Preset Register High
xD13	xD53	CTPRL	Counter/Timer Preset Register Low
xD15	xD55	CTCR	Counter/Timer Control Register
xD17	xD57	OMR	Output and Miscellaneous Register
xD19	xD59	CTH	Counter/Timer High
xD1B	xD5B	CTL	Counter/Timer Low
xD1D	xD5D	PCR	Pin Configuration Register
xD1F	xD5F	CCR	Channel Command Register
xD21-xD27	xD61-xD67	TxFIFO	Transmitter FIFO
xD28-xD2F	xD69-xD6F	RxFIFO	Receiver FIFO
xD31	xD71	RSR	Receiver Status Register
xD33	xD73	TRSR	Transmitter and Receiver Status Register
xD35	xD75	ICTSR	Input and Counter/Timer Status Register
xD37	xD77	GSR	General Status Register
xD39	xD79	IER	Interrupt Enable Register
xD3B	xD7B		Not used
xD3D	xD3D	IVR	Interrupt Vector Register - Unmodified
xD7D	xD7D	IVRM	Interrupt Vector Register - Modified
xD3F	xD3F	ICR	Interrupt Control Register
xD7F	xD7F		Not used

Appendix G Video Timing Parameters

The following table show the parameter values for some commonly used configurations. These values are for a NEC multisync monitor, but may be used for other terminals as well.

Table F-1 Video Timing Parameter Examples

Resolution	640 x 480	800 x 600	800 x 600	1024 x 768	1024 x 768	1280 x 1024
Ext Clock	5	5	5 or 8	5	8	8
PLL factor	5	7	8 or 5	13	8	13
Pixel freq.	25 MHz	35 MHz	40 MHz	65 MHz	64 MHz	104 MHz
HalfSync	12	9	10	8	8	13
BackPorch	12	18	30	33	30	52
Display	160	200	200	256	256	320
Short Display	61	76	58	88	91	117
BroadPulse	97	112	108	137	137	195
VSync	4	6	6	8	8	12
VBlank	79	32	32	38	38	52
VDisplay	960	1200	1200	1536	1536	2048
Linetime	198	248	284	336	330	408
MemInit	493	490	489	482	483	472
TransferDelay	19	22	23	30	29	40

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CC143 Product Note 02

To: CC143 Customers
Date: 21 September 1990
Subject: Known problems of CC143 with G300A and G300B chip

This product note provides a list of known problems with the CC143 module. All problems are realated to the G300 controller chip.

Both versions of the G300 chip (mask A and B) exhibit erratic behaviour. The following problems have been encountered.

1. Programming the chip after reset.
2. Access to the CLUT in byte-mode.
3. Distortion of video output signals.

1) The initialization method specified in the G300 data sheet and the CC143 technical manual (Version 1.1, page 5-10) does not work properly. A work-around for this problem has been found and is as follows for the G300A:

- Reset the G300A chip.
- Write the PLL multiplication factor to the Boot Location at address x683.
- Read a byte from the Boot Location at address x683.
- Read a byte from the Control register at address x583.
- Write the first byte to the Control Register (bits 7-0) at address address x583.
- Write the second byte to the Control Register (bits 15-8) at address address x583.
- Write the third byte to the Control Register (bits 23-16) at address address x583.

The initialization method for the G300B is as follows:

- Reset the G300B chip.
- Write the PLL multiplication factor to the Boot Location at address x683 (bit 5 must be written '1').
- Read a byte from the Control Register at address x583.
- Write the first byte (with value $80) to the Control Register (bits 7-0) at address address x583.
- Read a byte from the Control Register at address x583.

2) The CLUT cannot reliably be accessed in 8-bit mode when the VTG is running. The G300B Data Sheet Amendments (issue No. 1) states that a byte-access sequence must be aborted and restarted

when the G300 performs a Transfer (DMA) cycle before the access sequence has been completed. There is no method to detect if the G300 has made a Transfer cycle, other than performing a read sequence to check the written value. However this read sequence can also be interrupted by a G300 Transfer cycle which gives unreliable data. A method that may be used for accessing the CLUT is to wait for the FrameInactive signal to become True and then performing the three consecutive access cycles. This has the disadvantage that the FrameInactive signal must be polled and that interrupts should be masked when the processor performs the access sequence. During the first part of FrameInactive, the G300 has no need to start a Transfer cyle.

3) Distortion of the video output signals can be seen when using special screen patterns. The distortion is related to the signals on the PixData signal lines which are inputs for the G300. It seems that the PixData signals influence the analog output signals internal in the G300 chip. A redesign is planned by INMOS to solve this problem.