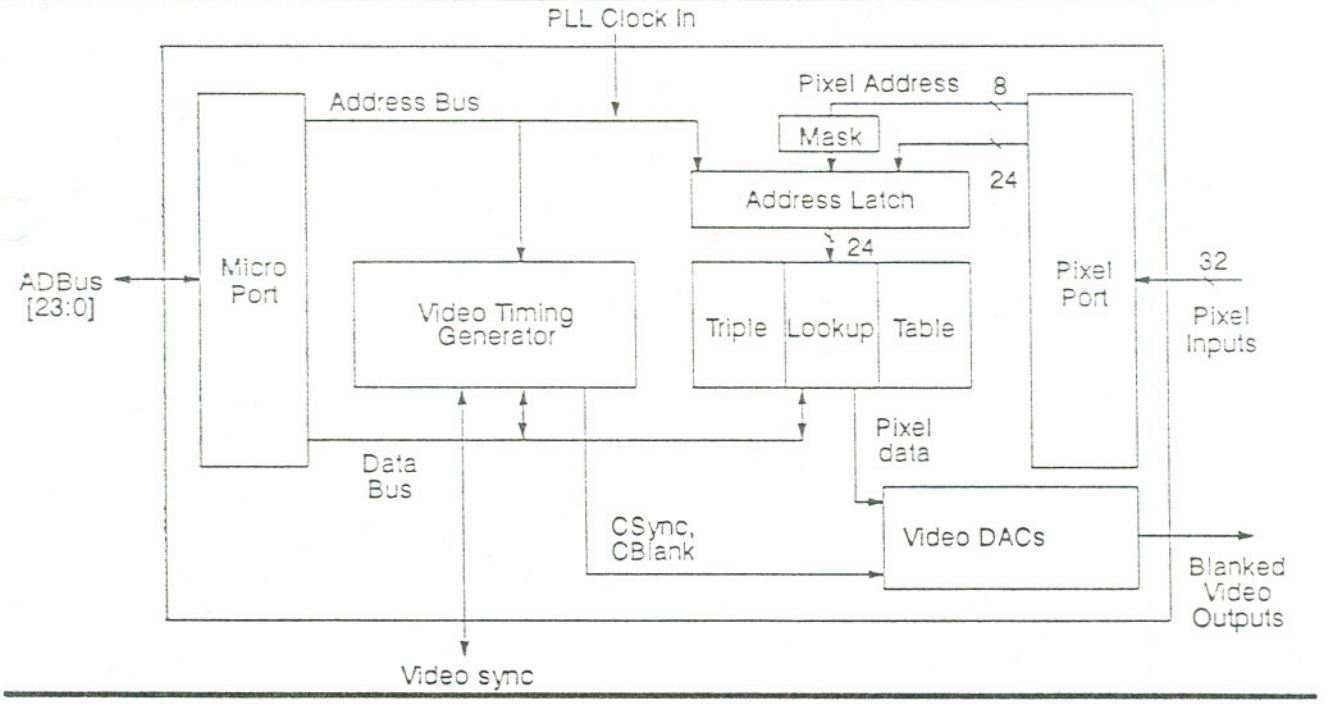
IMS G300B
colour video controller

inmos

Preliminary Data



FEATURES

Video rates up to 110 MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed Pixel input
1, 2, 4, 8 and 24 bit pixels
On chip triple lookup table
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible
Full colour mode with hardware gamma translation

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

SGS-THOMSON MICROELECTRONICS

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Contents

1.1 Introduction

The IMS G300 is a dedicated support chip which provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported video DRAMs. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data.

The device consists of a programmable video timing generator with screen refresh and auto line increment capability, a triple 256 location by 8 bit lookup table (LUT), a triple 8 bit video DAC and an on chip phase-locked loop (PLL); see figure 1.1.

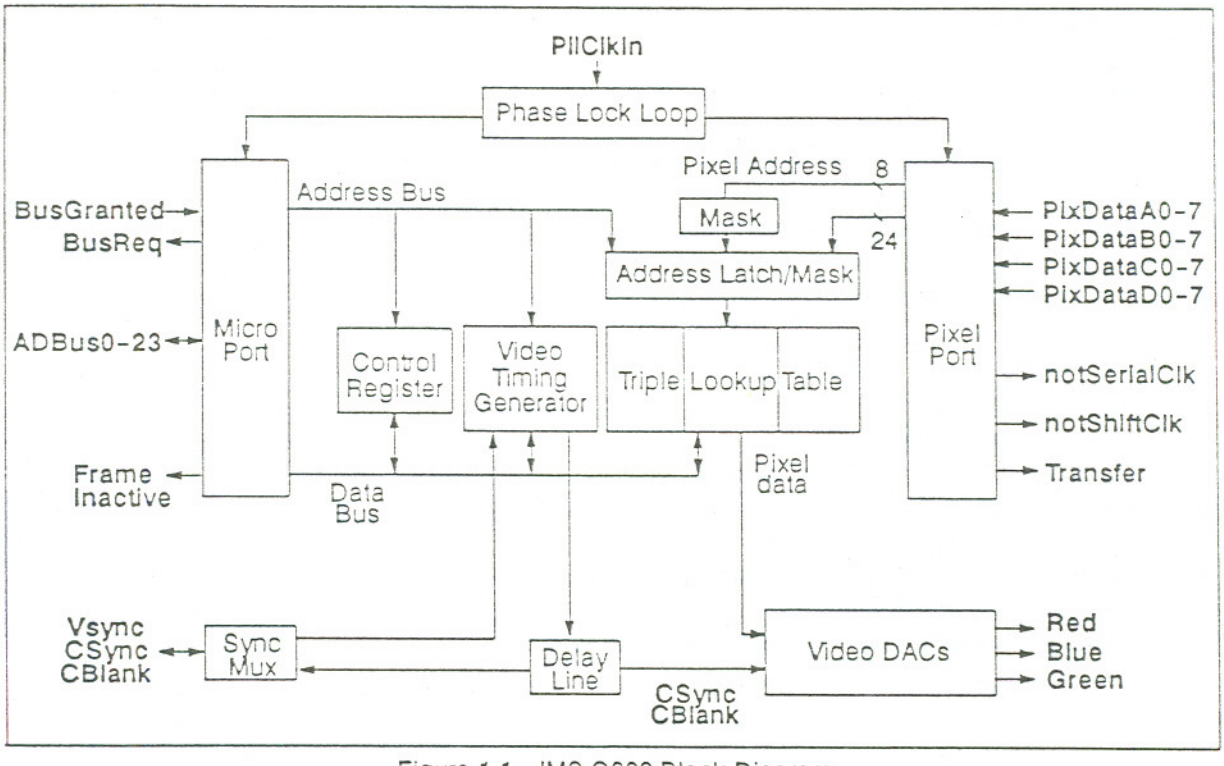

Figure 1.1 IMS G300 Block Diagram

1.1.1 Clocks

Use of the phase-locked loop allows the part to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

1.1.2 Video timing

The video timing generator is a programmable finite state machine which is programmed by loading a number of screen description parameters. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronising source which may be another IMS G300, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank and can supply tesselated or plain composite sync to the video DACs. The timing generator runs at one quarter of the video dot rate and the screen parameters are defined in terms of its resolution. Thus the screen is defined in multiples of four pixels.

1.1.3 Screen management

Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and which allows seamless mid-line update of the screen. The video RAM shift register can be made to

behave as though it is infinitely long and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at the appropriate times (a true serial clock output is also provided for system synchronisation). This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

1.1.4 Pixel port

The pixel port is 32 bits wide and has a number of operating modes, which are selectable in software.

In pseudo colour mode (mode 1), the 32 bit word can be interpreted as consisting of one, two, four or eight bit pixels. These are loaded at the relevant multiplex ratio and accelerated to the full dot rate before addressing the LUT. The 24 bits of pixel data thus accessed are then sent to the video DACs for display.

In full colour mode (mode 2), the top byte of the input word is ignored and the remaining three bytes are used as separate addresses into the triple LUT. No acceleration takes place before the data is sent to the LUT.

Mode 2 is usable only when an external dot-rate clock is supplied, mode 1 can also be used with the phase-locked loop.

1.1.5 Video DACs

The triple video DAC has 8 bit resolution at the full video rate and produces blanked video signals. It is possible to select various styles of analogue output to conform with generally approved monitor and broadcast television output levels and timings, including EIA-343 and CCIR.

1.1.6 Programming port

The IMS G300 has a memory mapped architecture which enables fast configuration and colour cycling through the use of block move or some other simple memory write cycle. Its micro-port appears as a block of memory (occupying 1/2Kword of address space) with the additional capability of operating in byte-wide or word-wide (24-bit) modes.

1.1.7 System Operation

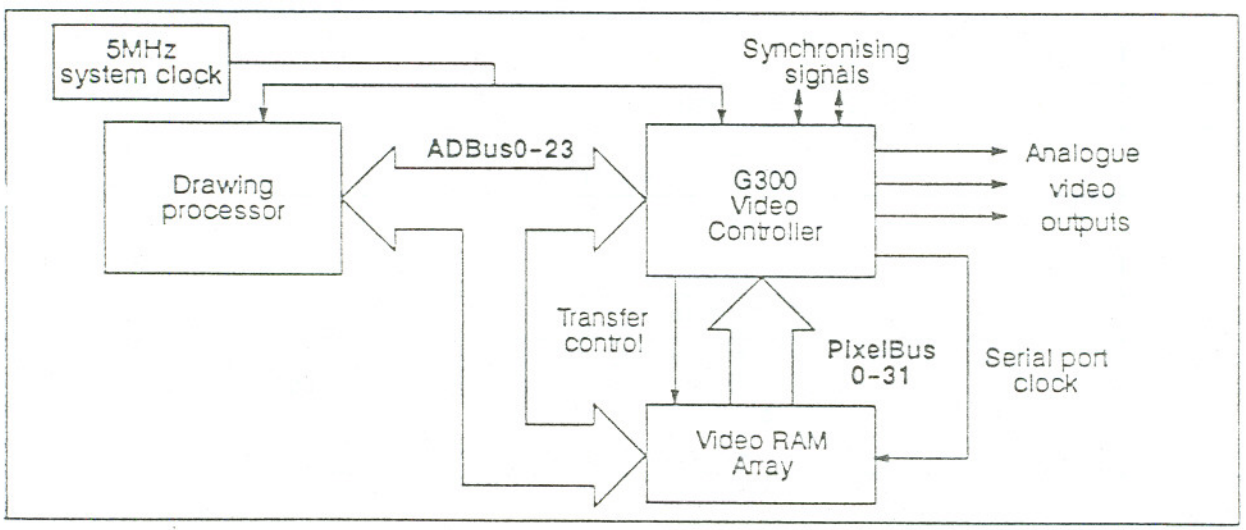

Figure 1.2 IMS G300 operating in a simple graphics system

Figure 1.2 shows how the IMS G300 would fit into a typical single-bitmap display system. The clock is sourced from a 5MHz crystal and the video data is being streamed to the screen at the full video rate of up to 110MHz. The video RAM array is directly accessed by the drawing processor and screen management is performed by the G300 on a DMA basis. All external digital signals and clocks are running at one quarter of the video rate.

1.2 Pin function reference guide

1.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	29	Timing signal which is high whenever the VTG is in Frame Flyback.
BusReq BusGranted	O I	26	DMA signals which, along with **Transfer**, supply the timing information to synchronously refresh the video ram shift registers.
ReadnotWrite notCS	I I	24	These signals provide all the timing information for accesses as well as defining access type.
ADBus0-23	I/O	24	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied to **ADBus2-11**. A byte-wide mode is available; the port is also used to drive out the 22-bit VRAM transfer address on **ADBus2-23**.

1.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk notShiftClk	O O	30	notSerialClk runs at one quarter the video frequency, notShiftClk varies its frequency depending on the bits per pixel required. Both of these clocks must be buffered.
Transfer	O	26	Transfer refreshes the video ram shift register synchronised to notSerialClk
CBlank	I	33	CBlank is a bidirectional blanking pin. Direction is soft selectable via control bit 16.
PixDataA0-7 PixDataB0-7 PixDataC0-7 PixDataD0-7	I I I I	30	The four pixel address bytes are used in the order A, B, C, D. In mode 2 **PixDataD0-7** is not used and RGB maps to ABC.

1.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	17	Active high, must be held active with clocks running for at least six cycles of notSerialClk.

1.2.4 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus CapMinus	N/A	38	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
ClkIn	I	11	Clock input for both PLL and times one operation.

1.2.5 Video signals

Pin name	I/O	Page No.	Comments
Red Green Blue	O O O	33	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	34	Video DAC reference current.
VSync CorHSync	I/O I/O	17	These pins can be used as outputs to supply various software-selectable sync signals or as inputs to lock the device to a system. They are both active low.

1.2.6 Supplies

Pin name	I/O	Page No.	Comments
AVdd	N/A	36	AVdd supplies analogue portions of chip.
Vdd	N/A	36	Vdd supplies digital portions of chip.
Ground	N/A	11	

1.3 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X1A0	23	Startup location to which must be written the clock multiplication factor and the clock source (PLL or dot rate).
Null	#1B0	25	Un-decoded location used for resetting byte mode state.
Top of Screen	#X180	25	Read/write register giving ability to reprogram the top of screen pointer at any time.
Control Register	#X160	5	Read/write control register. Read/write accessible at all times, contains all configuration information. Used to start and stop timing generator.
Mask Register	#X140	30	Read/write mask register. Read/write accessible at all times, masks each pixel address byte.
Datapath Registers	#X121 to #X12C	13	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Colour Palette	#X00 to #XFF	30	256 locations of 24 bit colours read/write accessible at all times, programmed via micro port. The values stored in the colour palette relate to the DACs as follows: lowest byte = RED, next byte = GREEN, highest byte = BLUE.

All other addresses in the range are reserved and must not be written to.

Note: #X = Hexadecimal address.

1.4 The control register and boot location reference guide

The bit pattern written to the control register determines the operating mode of the part. The function of each bit is given in table 1.1.

Bit	Function	Comments
23	Blank Function switch	1 = Undelayed ClkDisable at pad 0 = Delayed CBlank at pad
22	Reserved	Write zero
21	Interlace Standard	1 = CCIR Interlace format 0 = EIA Interlace format
20-19	Address step control	Sets size of VRAM transfer address increment
18-17	Bits per pixel	Sets Pixel port to required pixel depth
16	Blank I/O	1 = CBlank pin is output 0 = CBlank pin is input
15	Turn off blanking	1 = blanking disabled for test 0 = blanking enabled
14	Turn Off DMA	1 = No video RAM management 0 = DMA VRAM update operational
13	Reserved	Write zero
12	Black level	Selects blanking level 0 = Blank = Black level
11-9	Delay value	Delays Sync and Blank by 0 to 7 VTG clock cycles
8	Pixel port mode	0 = mode1, 1 = mode2
7	Micro port mode	0 = word mode, 1 = Byte mode
6	Reserved	Write zero
5	Analogue video format	1 = video only 0 = video and sync composite
4	Digital sync format	0 = mixed sync, 1 = separate sync
3	Frame flyback pattern	1 = plain synchronising waveform 0 = tesselated synchronising waveform
2	Device operating mode	0 = master mode, 1 = slave mode
1	Screen format	0 = non-interlaced, 1 = interlaced
0	Enable VTG	0 = VTG disabled, 1 = VTG running

Table 1.1 Control register bit allocations

Boot Address	Bit Allocation
#X1A0	ADbus6-23 = Write zero ADBus5 = Clock source select 1 = PLL mode, 0 = external clock mode ADBus0-4 = Binary coded PLL multiplication factor (when in external clock mode, load zero)

Table 1.2 Boot location bit allocations

1.5 Micro port timing reference guide

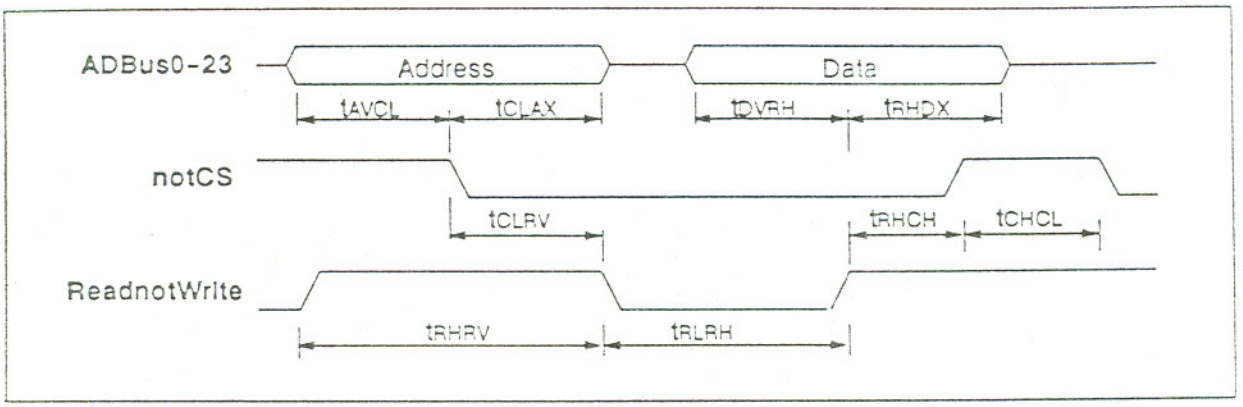

Figure 1.3 Micro port write cycle

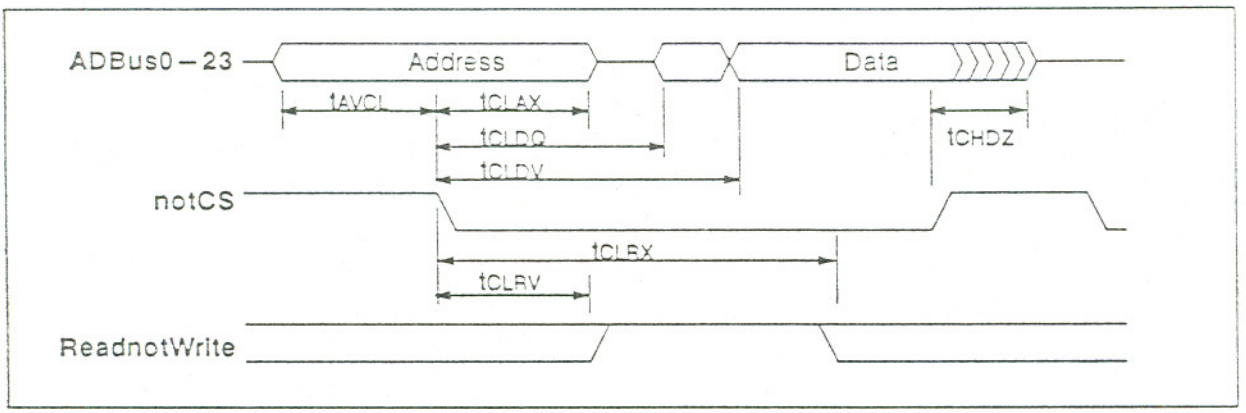

Figure 1.4 Micro port read cycle

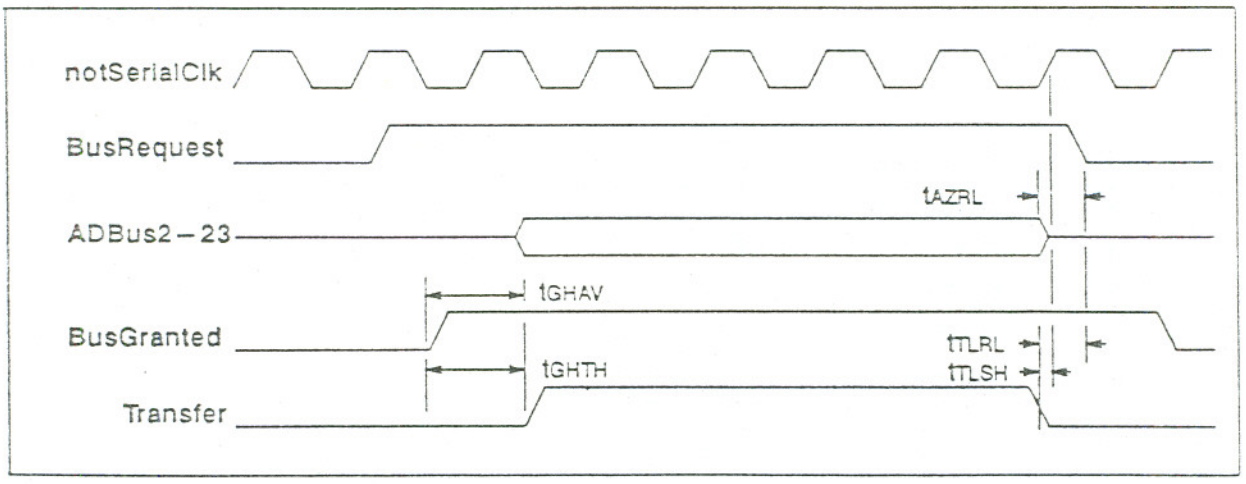

Figure 1.5 Micro port DMA and data transfer timings

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	10		ns
tCLAX	Address hold time	20		ns
tCLRV			0.5	periods SClk
tCHCL		1 + 20ns		periods SClk
tDVRH	Data setup time	10		ns
tRHDX	Data hold time	20		ns
tRHCH				*
tRLRH		4		periods SClk
tRHRV		1 + 20ns		periods SClk
tCLCL	Cycle time	7		periods SClk
Where SClk is the period of notSerialClk **Note:** These figures are not characterised and are subject to change				
RHCH = RHRV − CHCL − CLRV				

Table 1.3 Micro port write cycle parameters

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	10		ns
tCLAX	Address hold time	20		ns
tCLDQ	Time to bus driven	1.5		periods SClk
tCLDV	Data access time		5SClk + 20	ns
tCLRV			0.5	periods SClk
tCLRX		3.5 + 20ns		periods SClk
tCHDZ	Data turn off delay		30	ns
tCLCL	Cycle time	7		periods SClk
where SClk is the period of notSerialClk Note: These figures are not characterised and are subject to change				

Table 1.4 Micro port read cycle parameters

Symbol	Description	Min.	Max.	Unit
tGHAV	busGranted high to address valid		3*SClk + 30	ns
tAZRL	ADBus tristate to busRequest low	0		ns
tGHTH	busGranted high to Transfer high		25	ns
tTLRL	Transfer low to Bus Request low	1	2	SClk
tTLSH	Transfer low to notSerialClk high	−10	3	ns
Note: These figures are not characterised and are subject to change				

Table 1.5 Micro port DMA and transfer timing parameters

1.6 Pixel port timing reference guide

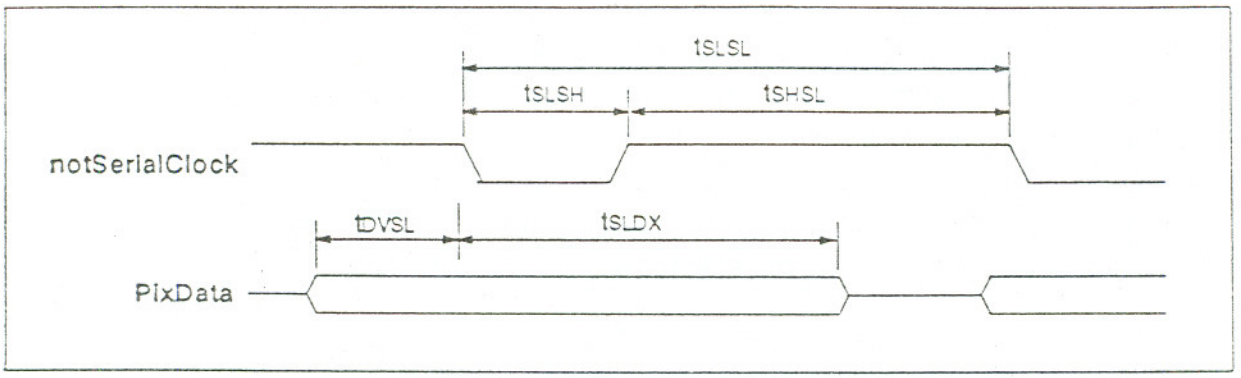

Figure 1.6 Pixel port signals in mode 1

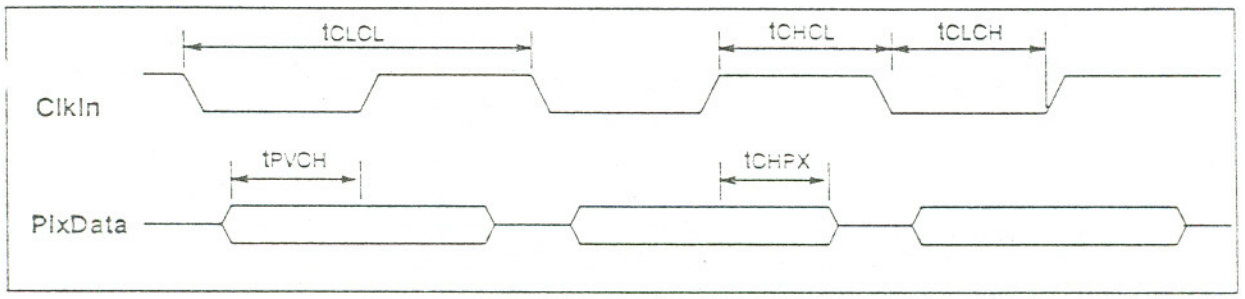

Figure 1.7 Pixel port signals in mode 2

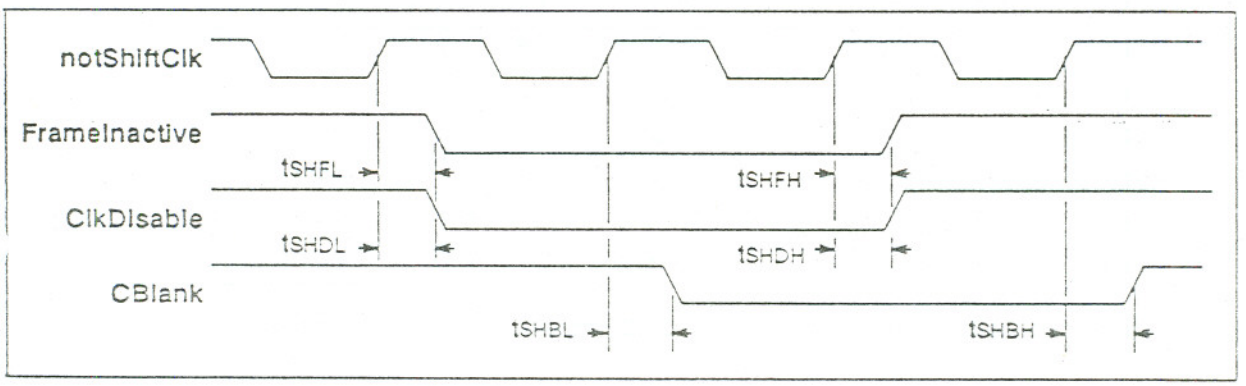

Figure 1.8 Relationship between notShiftClk, FrameInactive, ClkDisable and CBlank

Symbol	Description	-66 Min	-85 Min	-100 Min	-110 Min	Units
tSLSL	notSerialClk period	61	47	40	36	ns
tSLSH	Clk low time	12	10	10	10	ns
tSHSL	Clk high time	12	10	10	10	ns
tDVSL	data setup time	−3	−3	1	1	ns
tSLDX	data hold time	15	12	9	9	ns
Note: These figures are not characterised and are subject to change						

Table 1.6 Pixel port mode 1 timings

Symbol	Description	All Max	-66 Min	-85 Min	-100 Min	-110 Min	Units
tCLCL	Pixel period	10000	31	25	20	18	ns
tCHCL	ClkIn high time	10000	10	8	7	6	ns
tCLCH	ClkIn low time	10000	10	8	7	6	ns
tPVCH	Pixel data setup time		6	5	4	4	ns
tCHPX	Pixel data hold time		6	5	4	4	ns
Note: These figures are not characterised and are subject to change							

Table 1.7 Pixel port mode 2 timings

Symbol	Description	Min.	Max.	Unit
tSHFL		-5	5	ns
tSHFH		-5	5	ns
tSHDL		-5	5	ns
tSHDH		-5	5	ns
tSHBL		SClk/4-5	SClk/4+5	ns
tSHBH		SClk/4-5	SClk/4+5	ns

Table 1.8 **notShiftClk, FrameInactive, ClkDisable** and **CBlank** parameters

1.7 ClockIn timing reference guide

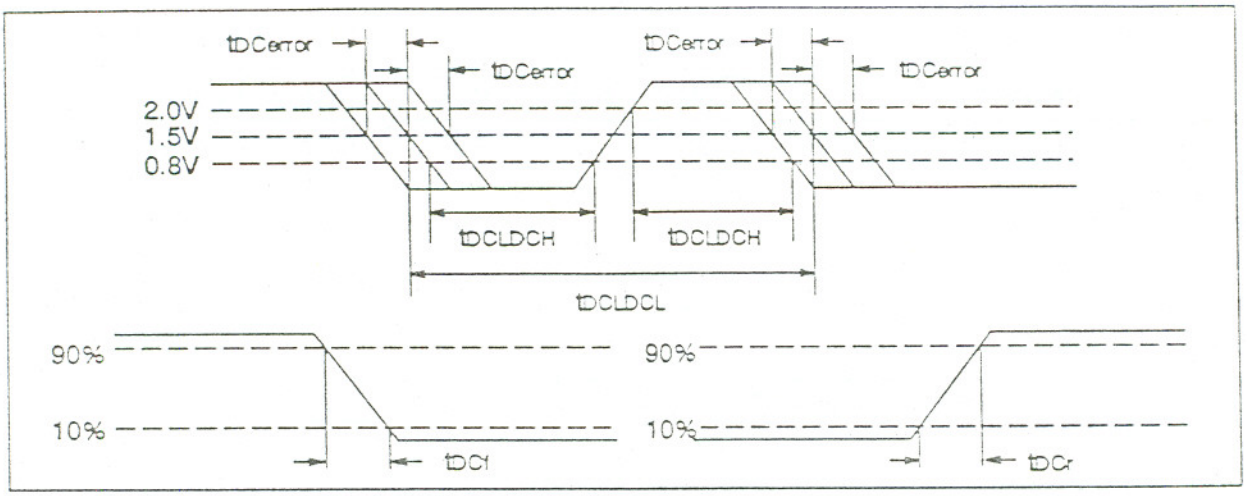

Figure 1.9 ClockIn timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
tDCLDCH	ClockIn pulse width low	20			ns	
tDCHDCL	ClockIn pulse width high	20			ns	
tDCLDCL	ClockIn period	100		200	ns	1
tDCerror	ClockIn timing error			±0.015	%	2
tDCr	ClockIn rise time			10	ns	3
tDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 1.9 ClkIn timings in PLL mode

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range VIH to VIL.

1.8 General parametric conditions and characteristics

1.8.1 Operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD + 0.3	Volts	
VIL	Input Logic '0' Voltage	−0.3		0.8	Volts	
TCPGA	Case Temperature	tbd		tbd	°C	2,3
TCQC	Case Temperature	tbd		tbd	°C	2,3
Note: These figures are not characterised and are subject to change						

Notes

1 AVDD = VDD

2 Measured on the lid of the package at maximum power dissipation.

3 VDD = 5V

1.8.2 Operating characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
IDD	Power Supply Current		250	tbd	mA	
IIN	Digital Input Current			±10	µA	
IOZ	Off State Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOH	Output Logic '0' Current	5			mA	
Note: These figures are not characterised and are subject to change						

1.8.3 Output drive capability

Parameter	Min.	Typ.	Max.	Units
notShiftClk			25	pF
notSerialClk			25	pF
Transfer			25	pF
ADBus [23:0]			25	pF

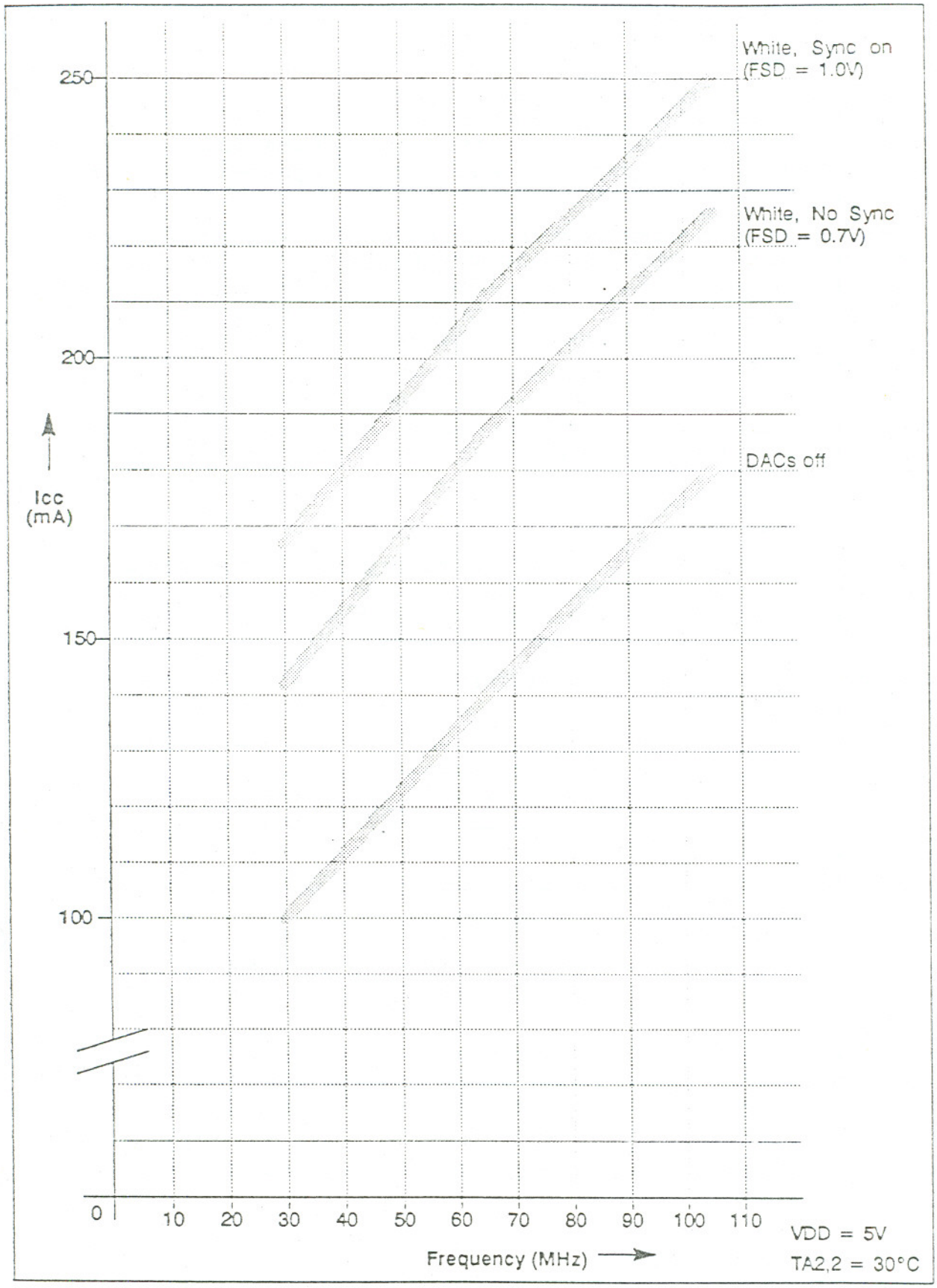

Figure 1.10 Icc (typical) versus pixel frequency

1.9 The video timing generator

1.9.1 Introduction

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **Transfer** and it starts and stops **notShiftClk** to control the flow of pixels onto the screen. It also provides a **FrameInactive** signal which is asserted whenever the display enters frame flyback, enabling the controlling processor to perform frame flipping or major screen updates invisibly.

The timing generator can be configured to control an interlaced or non interlaced monitor and to generate the synchronising waveforms required by the EIA-343 (NTSC) and CCIR (PAL) studio television standards. These options are selectable in software and are controlled by the contents of the control register. Also controlled by this register is the operating mode of the device; it can be set to free run in which case it will drive synchronising signals out, or it can be set into slave mode when it will lock onto frame and line sync pulses supplied externally.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each (i.e. a line with 1024 pixels is described as having 256 screen units).

1.9.2 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch plus line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

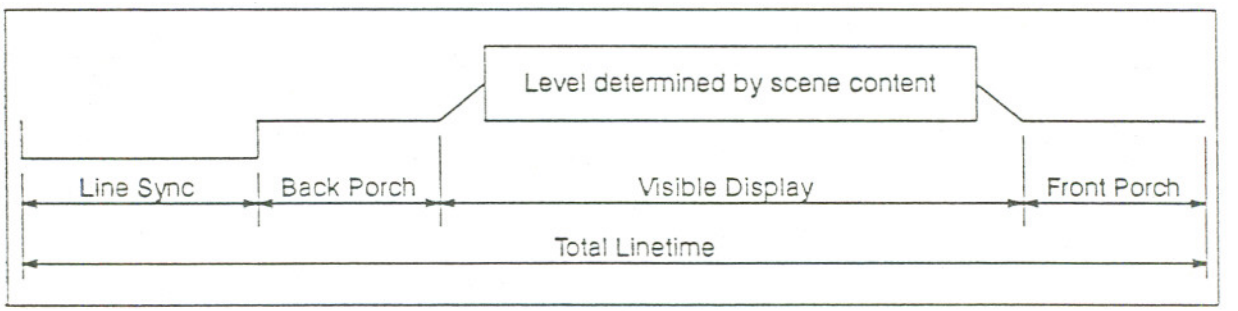

Figure 1.11 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure1.11. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels (equal to 256 screen units) is required, then 256 is the number written to the 'display' register. For the remainder of the scan, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 1.11 and this is the number written to the 'linetime' register.

1.9.3 Line timing parameters

The line segments shown in figure 1.11 map directly to timing generator registers with two exceptions. First, the line synchronising pulse is split into two periods of equal duration which are used in immediate succes-

sion – the parameter used for this is 'halfsync' – and second, there is no register for frontporch, rather the total line time is programmed into a separate register and the end of the scan line occurs when this time-base period expires.

Figure 1.12 (a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on which part of the cycle is being executed.

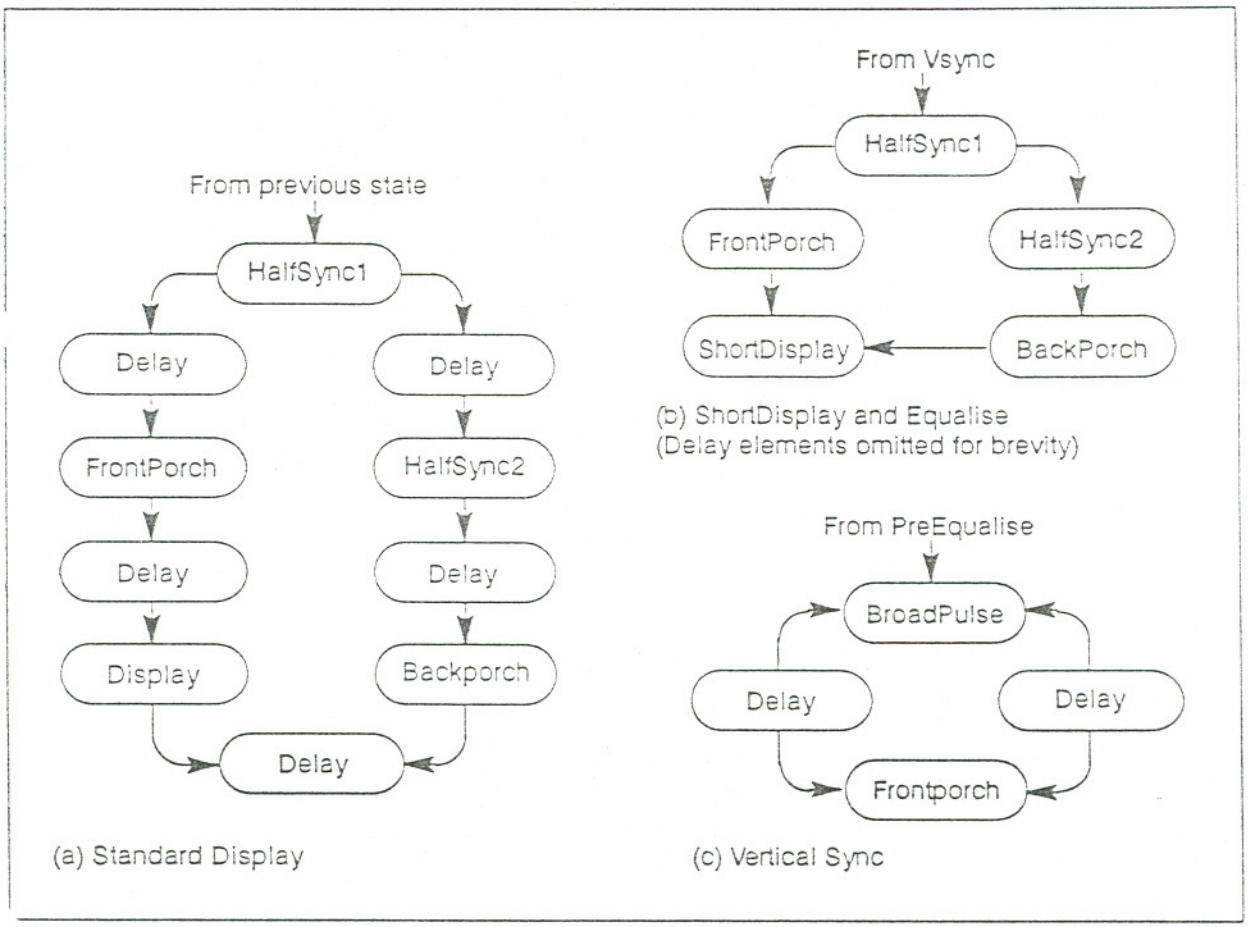

Figure 1.12 Flow diagrams for video timing generator

Figure 1.13 (a) shows the relationship of the screen description parameters to a full scan line. Note that frontporch is undefined and halfsync is used twice in succession to construct the line sync pulse.

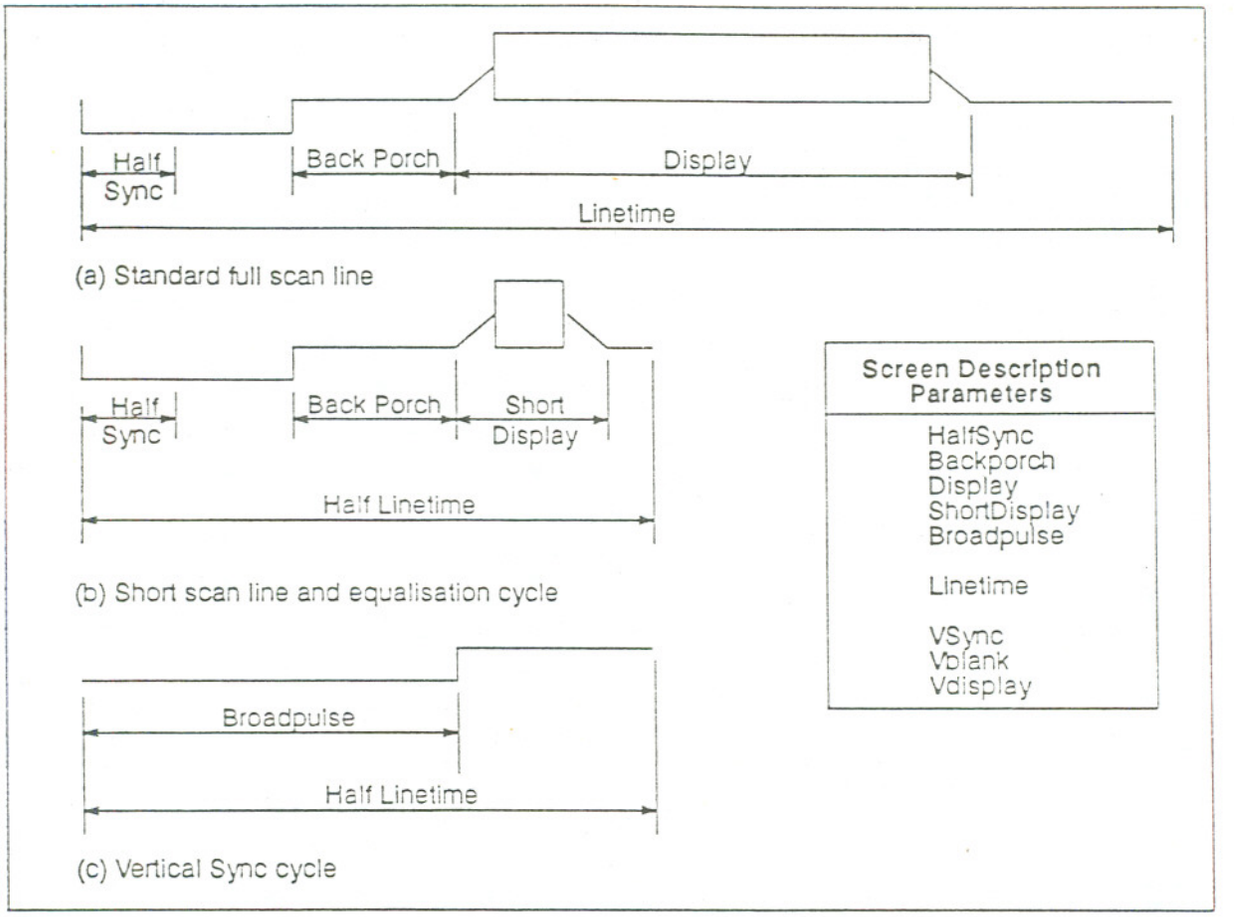

Figure 1.13 Screen description parameter definitions

1.9.4 Frame timing parameters

The G300 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 1.14).

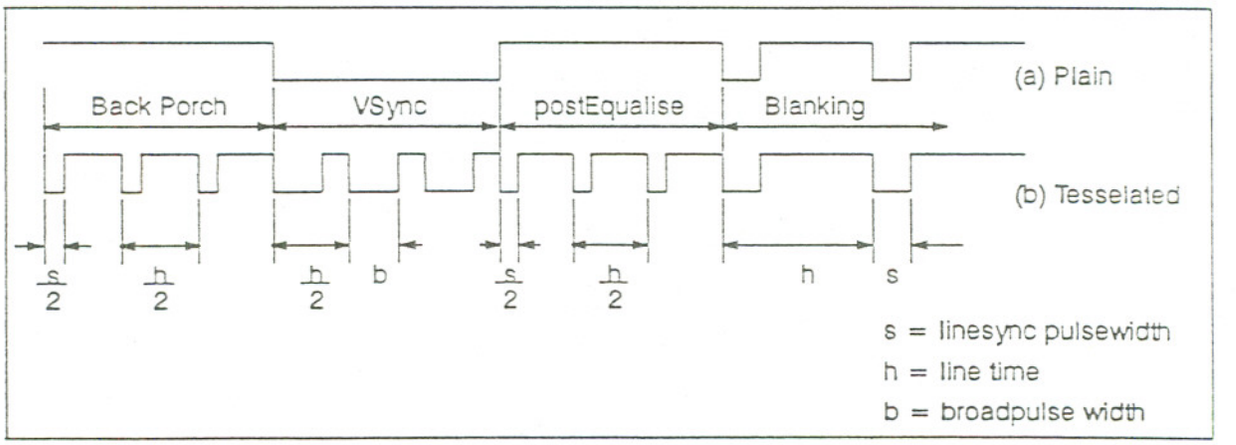

Figure 1.14 Composite Sync frame flyback waveforms

A further requirement of the television standards is that each frame must contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-in-

erlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of 625 lines would have 625 in that register since in interlace, the VDisplay register decribes the vertical display *field* rather than the entire frame – see table 1.10).

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	illegal	illegal
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 1.10 Frame programming examples

The duration of preEqualise, postEqualise and VSync are all set by the VSync parameter and are hence always equal, the vertical backporch period is independent and has its own parameter, Vblank. The total frame blanking period is the sum of these four.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 1.14(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Reference to figure 1.12(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

1.9.5 Parameter calculation

Calculation of the frame timing parameters is simple and direct – to produce the flyback waveform in figure 1.14(a) the parameter VSync is set to 3 – and the line parameters are derived from the equations in table 1.11. There is also an example in section 1.17.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	BackPorch
Display	=	Display
Linetime	>	(2×HalfSync + BackPorch + Display)
During an equalisation cycle		
ShortDisplay	<	Linetime/2 – (2×HalfSync + BackPorch)
Low period	=	HalfSync
High period	=	Linetime/2 - HalfSync
During a VSync cycle		
BroadPulse	=	Linetime/2 - Pulse width*
Low Period	=	BroadPulse
High period	=	Pulse width

Table 1.11 Screen description line parameter equations

* Note: Pulse width = duration of serration pulse high time

The following restrictions on parameter values must be observed:

- All parameters must be non-zero.
- Linetime must be an even multiple of the period of notSerialClk.
- 2×HalfSync + BackPorch + Display > Linetime/2 > 2×HalfSync + BackPorch.
- The total number of displayed lines in each frame must be a whole number. In interlace, this must be an odd whole number.
- Backporch must exceed TransferDelay by at least one notSerialClk period.
- Transfer delay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 1.12).

1.9.6 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G300 bootstrap location. The effect of this is to set the PLL multiplication factor and clock source (PLL or external crystal). Following this it must set the micro-port mode (byte wide or word wide) by writing to bit 7 in the control register and initialise the VTG by writing a 0 to bit 0.

Startup sequence:

4 Assert, then deassert Reset.

5 Write configuration pattern to bootstrap location.

6 Write to control register to set microport and initialise VTG.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG which will then start up immediately at the beginning of frame sync. The G300 can be reprogrammed without asserting Reset.

The reprogramming sequence has three steps:

1 Write zero to bit 0 of the control register, disabling VTG.

2 Write to the screen parameter registers chosen for redefinition.

3 Write one to bit 0 of the control register, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

1.10 The G300 Address Map

The various register locations of the IMS G300 are memory mapped as shown in the table below. The values given are hexadecimal word addresses driven on to ADBus2-10 All other locations within the address space occupied by the G300 are reserved and must not be addressed. The boot location is not readable, all other locations are read/write.

Location	Address
Colour Palette	
starts	#X000
ends	#X0FF
Mask Register	#X140
Control Register	#X160
Top of Screen	#X180
Boot Location	#X1A0
Data Path Registers	
HalfSync	#X121
BackPorch	#X122
Display	#X123
ShortDisplay	#X124
BroadPulse	#X125
VSync	#X126
VBlank	#X127
VDisplay	#X128
Linetime	#X129
Top of Screen	#X12A
MemInit	#X12B
TransferDelay	#X12C

Table 1.12 IMS G300 address map

1.11 Synchronising and Blanking signals

1.11.1 Introduction

The video timing generator produces sync and blank signals to a pattern specified by a combination of the operating mode of the G300 and the screen description parameters. Internally, composite sync and composite blank are supplied to all three video DACs by default. However, both of these functions can be disabled by setting bits 5 and 15 of the control register, respectively.

The internal sync and blank signals are supplied with the correct delay to allow for the transfer of data from the video RAM array into the G300 with the difference in delay due to the alternate G300 operating modes automatically catered for.

In order to allow pipeline stages between the output of the video RAM and the pixel inputs , the IMS G300 includes a programmable delay line which can be set (via Control Register bits 9 to 11) to insert a further delay of up to seven **notSerialClock** cycles between the outputs of the VTG and the inputs of the DACs.

1.11.2 Master mode

When running in master (internal sync) mode, the **VSync** and **CorHSync** pins are outputs and the G300 drives them in the appropriate fashion, active low. Composite or Horizontal sync selection is specified by Control Register bit 4. Untesselated frame sync always appears on the **VSync** pin while the **CorHSync** pin is switchable to supply one of Line sync, untesselated composite sync or tesselated composite sync (see table 1.13). These signals are all delayed by the same amount as the internal sync signals specified above. They are also subject to the further delays as programmed into the control register.

Control Bits		Vsync	CorHSync	
			HSync	CSync
4	3			
0	0	Plain	-	Tesselated
0	1	Plain	-	Plain
1	0	Plain	Plain	-
1	1	Plain	Plain	-

Table 1.13 Sync Style Selection

1.11.3 Slave mode

In slave mode the **VSync** and **CorHSync** pins are designated as inputs and the G300 will lock onto vertical and horizontal sync pulses supplied to them.

The sampling circuit on the **Sync** inputs means that the IMS G300 can be locked to a completely asynchronous source without metastability problems. It will tolerate a large amount of instantaneous variation in the synchronising inputs due to the inbuilt flexibility of the timing algorithm. This provides synchronisation guaranteed to within one period of **notSerialClk**, which may not be adequate in a system where two video streams are being merged. In this case, it is necessary to observe the timing shown in figure 1.15 when the G300 will give no synchronising errors.

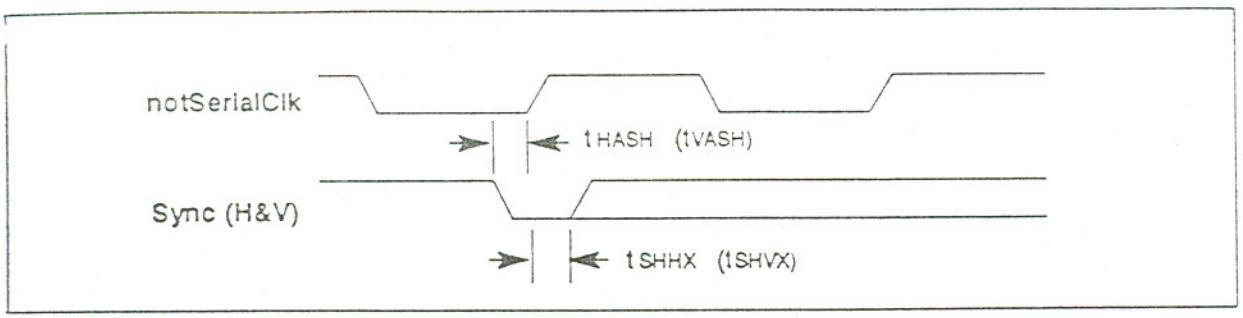

Figure 1.15 External synchronisation

For a genlocked system, it will be necessary to run the G300 in external clock mode (ie: not using the phase locked loop) with **ClkIn** derived from the global linesync using a standard sync splitter and external PLL.

When set to slave mode, the G300 will free run until it recieves a frame sync signal which resets the timing generator to the start of **VSync**. There will be a fixed delay between the **VSync** signal being detected and the VTG restarting. This delay will remain constant from then on. In an interlaced system, the G300 will sample the line sync pulses to determine the current field and, on detecting an error, it will resynchronise at the start of the next field, thus there may be a period of one field duration before a correct lock is achieved. In order to function correctly, the external line sync pulse must overlap by at least one period of **notSerialClk** with the internally produced line sync.

Symbol	Description	Min.	Max.	Unit
tVASH	Vsync setup time	SClk/4	3SClk/4	ns
tHASH	Hsync setup time	SClk/4	3SClk/4	ns
tSHVX	Vsync hold time	0		ns
tSHHX	Hsync hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 1.14 External sync waveform timings

1.11.4 Digital Blanking pin

The **CBlank** pin is configured by bit 16 of the Control Register to be input or output. As an input it is treated in exactly the same way as a pixel thus in mode 1 its resolution varies from every fourth pixel boundary at 8 bits per pixel to every 32nd pixel boundary at one bit per pixel. In mode 2 it is sampled along with each pixel latched in. The input data on this pin has the same timing requirements as a Pixel input.

As an output, **CBlank** has two distinct possible functions which are selected by bit 23 of the Control Register. Function one is as a simple blanking output, active high and delayed to coincide with the blanking period of the DAC outputs. Function two is as a clock disable pin. This is undelayed with respect to **notShiftClk** and has special behaviour at the start of an even interlace field. Whereas composite blank is active during the first half of the first scan line of an even field, clock disable is not, so that the requirements of the VRAM framestore can be met. The purpose of this function is to stop and start the pixel clock in a system which uses less than 4:1 multiplexing in the video RAMs, as is possible in mode 2 operation.

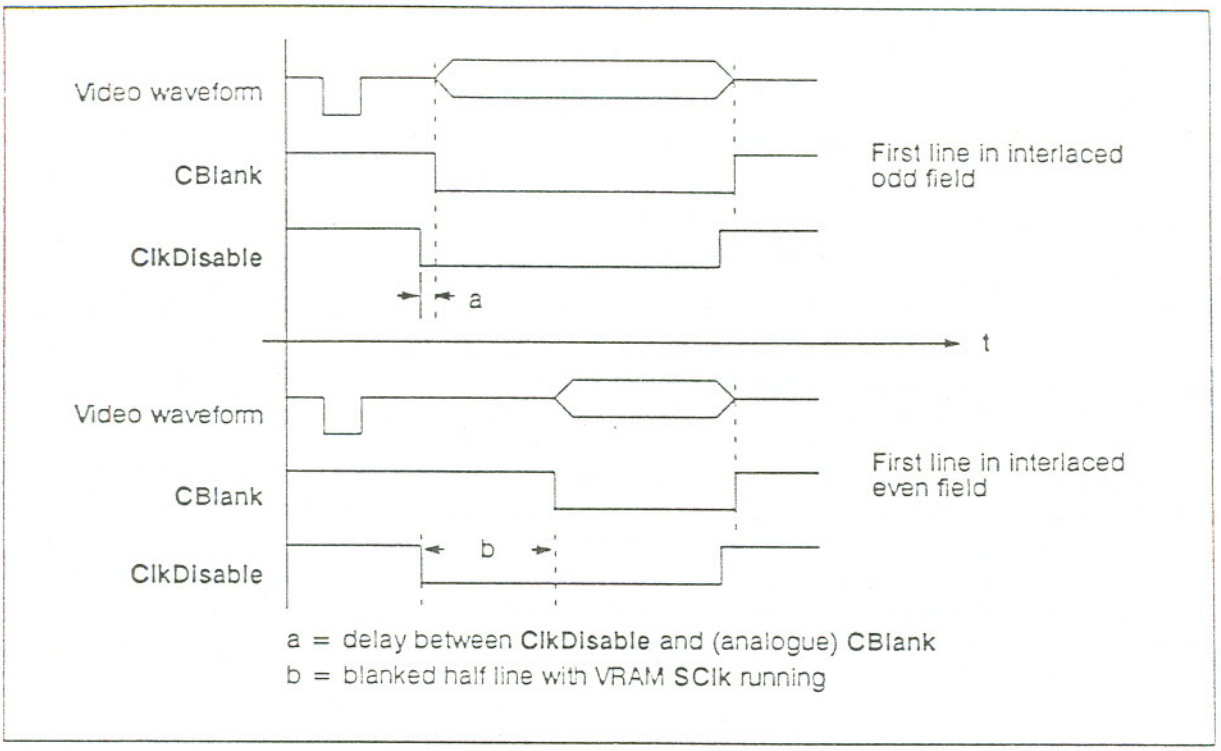

Figure 1.16 Relationship between Video, CBlank and ClkDisable

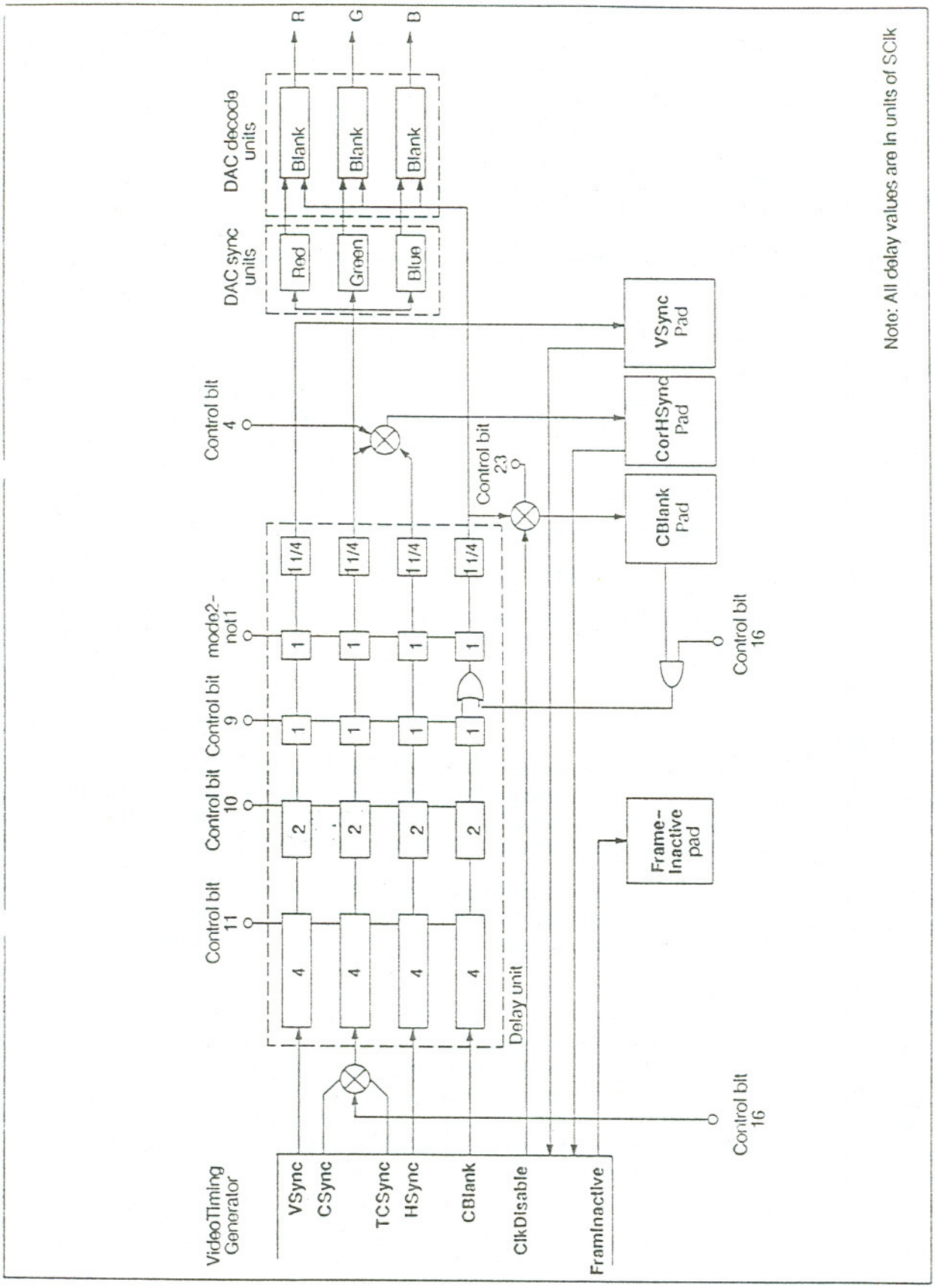

Figure 1.17 Digital and analogue syncing and blanking system

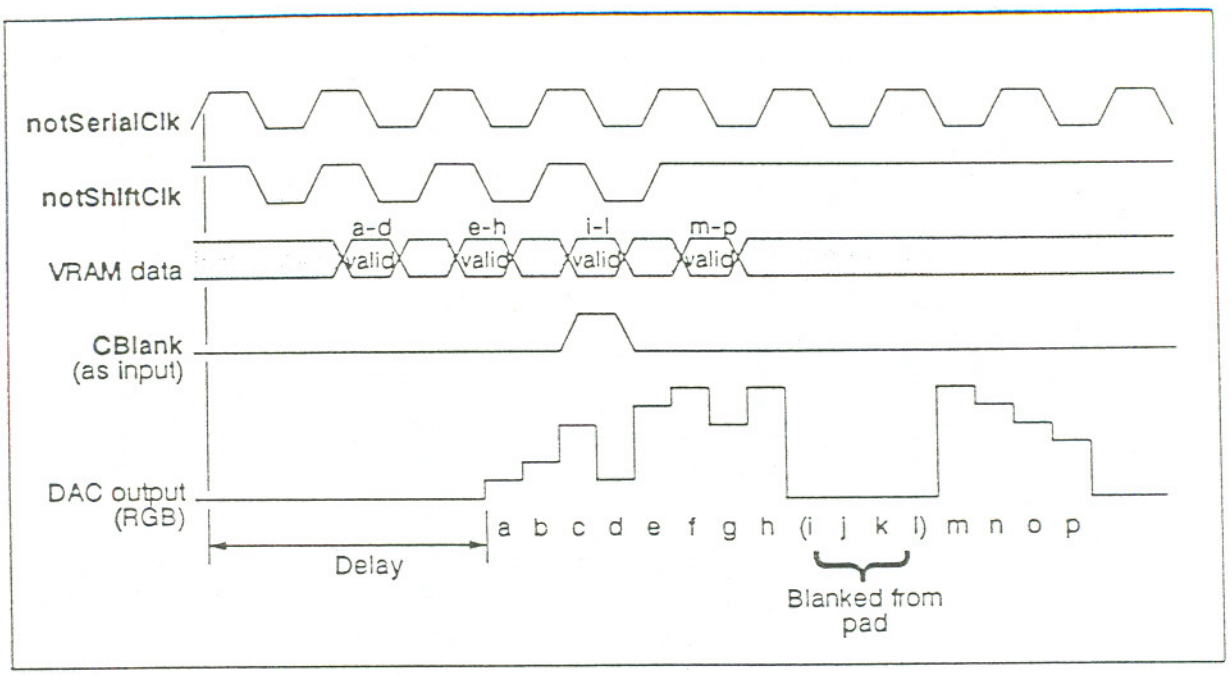

Figure 1.18 Delay between **notShiftClk** and DAC outputs in mode 1

$$\text{Delay} = \text{SClk} \times (2.5 + 4 \times \text{Control bit 11} + 2 \times \text{Control bit 10} + 1 \times \text{Control bit 9})$$

Note: Diagram shows delay with Control bits 9 to11 = 0

1.12 The micro port

1.12.1 Introduction

The micro port is a bidirectional 24 bit interface which can be configured to operate in byte wide or 24 bit wide mode (word mode). It consists of a multiplexed address and data bus with several control signals, described below, and is used for programming both the video timing generator screen description registers and the colour lookup table. The micro port timings are asynchronous with the remainder of the G300.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaken DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

1.12.2 Initialisation

The choice of clock source is made by writing to bit 5 in the boot location. If the phase locked loop is to be used, a suitable crystal oscillator must be connected to the **ClkIn** pin. If the direct drive option is used, the system must supply a dot rate clock to the **ClkIn** pin. On Power up, the **Reset** pin must be taken high and ClkIn must have been running for at least t_{CVRL} after **Vdd** is valid before the end of **Reset**. After deasserting **Reset**, the first access to the micro port must be a preliminary configuration access to the boot location as specified in section 1.9. This sets the clock source and the PLL multiplication factor if the clock source is to be the PLL.

The microport mode defaults to word mode on reset so, if byte wide operation is required, it must be selected by writing to bit 7 in the control register.

Once these two write cycles have been performed normal operation of the micro port may commence.

1.12.3 Programming operation

For normal read and write cycles the address is latched into the G300 on the falling edge of notCS. ReadNotWrite is sampled 1/2 a period of notSerialClk later to establish the cycle type. In a read cycle, the data lines will be driven a time tCLDV later and will remain valid until notCS goes high. In a Write cycle, data will be latched into the G300 on the rising edge of either ReadNotWrite or notCS, whichever occurs first.

1.12.4 Byte Wide operation

When the part is configured to byte-wide mode, three complete read or write cycles must be made to the same address in order to complete each cycle. The data is written to or read from ADBus0-7 least significant byte first. A byte wide read or write may be aborted before completion without causing data corruption. The system is reset by latching in a new address.

Read cycles

The micro port stores a history of accesses using a three-deep buffer. For every Read cycle, it determines whether the last access was a read, and if so, whether it was from the same address. If the last access was a write, or if it is was from a different location to the current read, then an internal 24-bit data fetch is performed and the least significant byte is driven out onto ADbus 0-7.

If the current read is from the same address as an immediately preceding read, the data stored from that previous internal data fetch is rotated eight bits and the next most significant byte is driven onto ADbus 0-7.

Write cycles

For a Write cycle, the data presented to ADbus 0-7 is stored until the micro port detects the third write to the same address, when an internal data store is performed. If a byte write sequence is aborted before completion by either writing to a different address or by performing a read, then no data will have been written due to that operation.

Writing to the Control register in byte mode

The control register is a special case in that the access history must be reset between two consecutive accesses to its address. This is done in the normal way by performing an aborting cycle.

Thus two control register writes must be separated by either a read or a write to some other location.

Address #X1B0 is a suitable address for Null accesses.

Interaction with DMA

The byte access history registers are completely static so that there is no overall time limit for completion of a byte access. However, if the G300 completes a DMA cycle before a byte access sequence has completed, then that cycle must be aborted and restarted.

Aborting a byte-access sequence

A read access sequence is aborted by performing a write, and a write access sequence is aborted by performing a read. If the access is being aborted to perform a sequence of the other type then the aborting access can be from the first access of a sequence. If the aborted access is to be restarted immediately then the aborting access is itself aborted by the restarted operation.

Initialising to byte mode

Since the G300 defaults to word mode, the control register access to set the microport to byte mode is an exception to the above rules. It must be aborted after a single access, before normal operation commences. If the access immediately following it is to be a read, that is sufficient to initialise the byte sequencer – but a single read operation must be inserted if the next access is a write.

1.12.5 Byte access sequence definitions

Definition	Notes
a) Write to control register to configure micro port to byte mode	
1 Write to #160, setting bit 7 to 'one'	
2 Read from #1B0	
3 Commence normal byte operations	
b) Normal byte write sequence	
1 Write to address #A, driving least significant byte of word onto ADBus0-7	
2 Write to address #A, driving next significant byte of word onto ADBus0-7	
3 Write to address #A, driving most significant byte of word onto ADBus0-7	
c) Normal byte read sequence	
1 Read from address #A, reading least significant byte of word from ADBus0-7	
2 Read from address #A, reading next most significant byte of word from ADBus0-7	
3 Read from address #A, reading most significant byte of word from ADBus0-7	
d) Normal byte access to/from control register	
1 Perform normal read or write sequence as defined above to/from address #160	
2 Perform normal read or write sequence to/from address #1B0	1
e) Aborted byte write sequence	2
1 Perform steps 1, or steps 1 and 2 of Normal byte write	
2 Either : i) Write to any address except #A or ii) Read from any address	
f) Aborted byte read sequence	2
1 Perform steps 1, or steps 1 and 2 of Normal byte read	
2 Either : i) Read to any address except #A or ii) Write from any address	

Notes

1 This step can be replaced by either:
i) A single read/write from any location except #160
or:
ii) A valid byte read/write sequence from any valid location.

2 The aborting read or write may be the first operation of a valid byte read or write sequence.

1.12.6 The transfer address, line start and top of screen

The G300 outputs a new 22 bit address on ADBus2-23 during every transfer cycle it initiates. The first address in each frame is specified in the Top of Screen register, which is programmed on startup but which can be modified at any time. Note that this register appears at two separate locations, Line Start and Top of Screen. Line Start is accessible only when the VTG is disabled, Top of Screen, only when it is running.

The current row address is incremented by the amount specified in bits 20–19 of the control register, used in conjunction with the 'Interlace' bit (bit 2). These bits specify the VRAM step length and the screen format. Refer to table 1.15. for bit assignments.

The column address is never incremented by the G300 so that the SAM start address remains constant until modified by the host.

Changes to the Top of Screen pointer become effective from the top of the subsequent screen (or field in an interlace system).

The framestore format for interlace is identical to that for non-interlace. Address ordering depends on the standard selected. CCIR scans even lines first, NTSC scans odd lines first.

In interlace, the first half of Line Zero is always blanked at the video DACs but the G300 will clock the VRAM shift registers as though visible. This preserves compatibility between interlace and non-interlace.

Option	Register Bit			Description
	20	19	1	
a	0	0	0	Increment by 1. Non interlace format. Maintains compatibility with equivalent G300A mode.
b	0	0	1	Increment by 1. Interlace format.
c	0	1	0	Increment by 256. Non interlace format.
d	0	1	1	Increment by 2. Interlace format. Replaces G300A interlace mode. Every second field offset by 1.
e	1	0	0	Increment by 512. Non interlace format.
f	1	0	1	Increment by 512. Interlace format. Every second field offset by 256.
g	1	1	0	Increment by 1024. Non interlace format.
h	1	1	1	Increment by 1024. Interlace format. Every second field offset by 512.

Table 1.15

1.12.7 The screen transfer operation

The G300 provides two software programmable strobes which enable it to perform the necessary screen data-transfer cycles on video RAMs to reload the internal shift registers with new data. These may be synchronous updates which happen part way across a line or updates which occur during flyback.

The user may program these strobes, **BusRequest** and **Transfer**, to cause the data transfer cycles to occur at the correct points during the screen display to implement seamless line update, thus decoupling the screen configuration from dependence on the video RAM architecture. These strobes are controlled by values loaded into two special purpose registers, MemInit and TransferDelay. The G300 also outputs a transfer address specifying the new row of pixels to be displayed. It is left to the user to generate RAS, CAS and any other strobes he may need from **busRequest**, **Transfer**, **notSerialClk** and **notShiftClk**.

The G300 is primarily designed to be used with video RAMs, although it can be used with static or standard dynamic rams if desired. In this case the strobes provided can be used to arbitrate bitmap accesses.

1.12.8 Transfer cycle timing

Video RAMs reload their shift registers by performing a normal read cycle with a special pin (usually called notDT or notDT/notOE) held low as RAS falls. The address values presented to the VRAM on the falling edges of RAS and CAS define which row is loaded into the shift register and which bit in the shift register is shifted out first, respectively. The instant at which the actual transfer takes place is set by the time at which notDT is brought high again and this edge alone must be synchronised to the shift clock which clocks data out of the shift registers.

In many systems the reloading of the shift registers takes place at the end of the line during retrace. However, one of the most useful features of using the G300 with VRAMs is the ability to reload the shift registers mid-line. This allows screens with an arbitrary number of pixels per line to be constructed with any length shift register. In order to do this however some look-ahead is required in order to be able to make the transfer at exactly the right point without any discontinuity on the screen. This look-ahead is provided by programming the appropriate values into the MemInit and TransferDelay registers.

At the start of each display frame, the G300 will initiate a transfer cycle at the beginning of the backporch period of the first line and will perform the data transfer with the delay specified in the TransferDelay register.

This ensures that there is data loaded ready for the first line scan to begin.

The G300 will then begin to count **notSerialClk** cycles and will initiate a further transfer cycle after MemInit cycles of **notSerialClk** by asserting **BusReq**. After a further number of cycles of **notSerialClk** equal to TransferDelay, the G300 will take **Transfer** low and the new data will be loaded into the shift registers.

TransferDelay	$\leq$	Backporch -1
TransferDelay	=	System DMA Latency + VRAM Access + 4 SClk
MemInit + TransferDelay	$\leq$	VRAM shift register length - SAM start address
		In an interlaced system only:
MemInit + TransferDelay	=	Display
TransferDelay	<	ShortDisplay

Table 1.16 Restrictions of screen update parameters

Thus the period of row transfer operations is;

MemInit + TransferDelay

and apart from the restrictions quoted above, it need bear no relation to the screen line length at all. This permits any display line length with any type of video RAM.

The critical parameter as far as DMA accesses are concerned is TransferDelay which needs to be long enough to allow for the DMA latency of the drawing processor as well as the access time of the video RAMs. The G300 imposes an extra overhead of one notSerialClk period which needs to be added to the Transferdelay parameter but which does not appear as part of the delay between **BusReq** and notDataTransfer.

If there is a data transfer operation pending when the system enters flyback, (i.e. the G300 would have control of the bus for a considerable length of time) then the transfer cycle is aborted before **BusReq** is made and will be restarted on the next following active display backporch. This ensures that any DRAM is never left unrefreshed during flyback and also makes best use of the available memory bandwidth. In order to implement this function, the G300 predicts, after a DMA is internally sheduled but before BusReq is asserted, that the video RAM shift registers are not going to run out of pixels before the end of the current line and hence the Row refresh may be left until the following active backporch. When **BusReq** is rescheduled the DMA is restarted at the beginning of backporch in the same way as the first line in the frame but the transfer delay parameter is carried over from the previous line and is incremented only when the system re-enters active display. This preserves the correct ordering of data onto the screen, while the insertion of the backporch period ensures that the DMA latency is always exceeded. Refer to figure 1.20 .

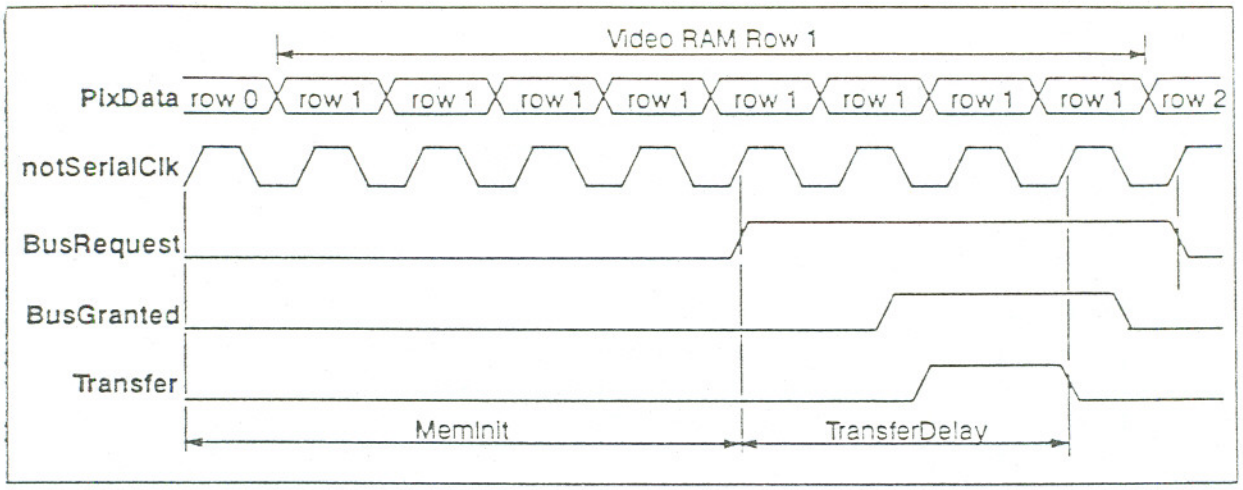

Figure 1.19 Data transfer sequence

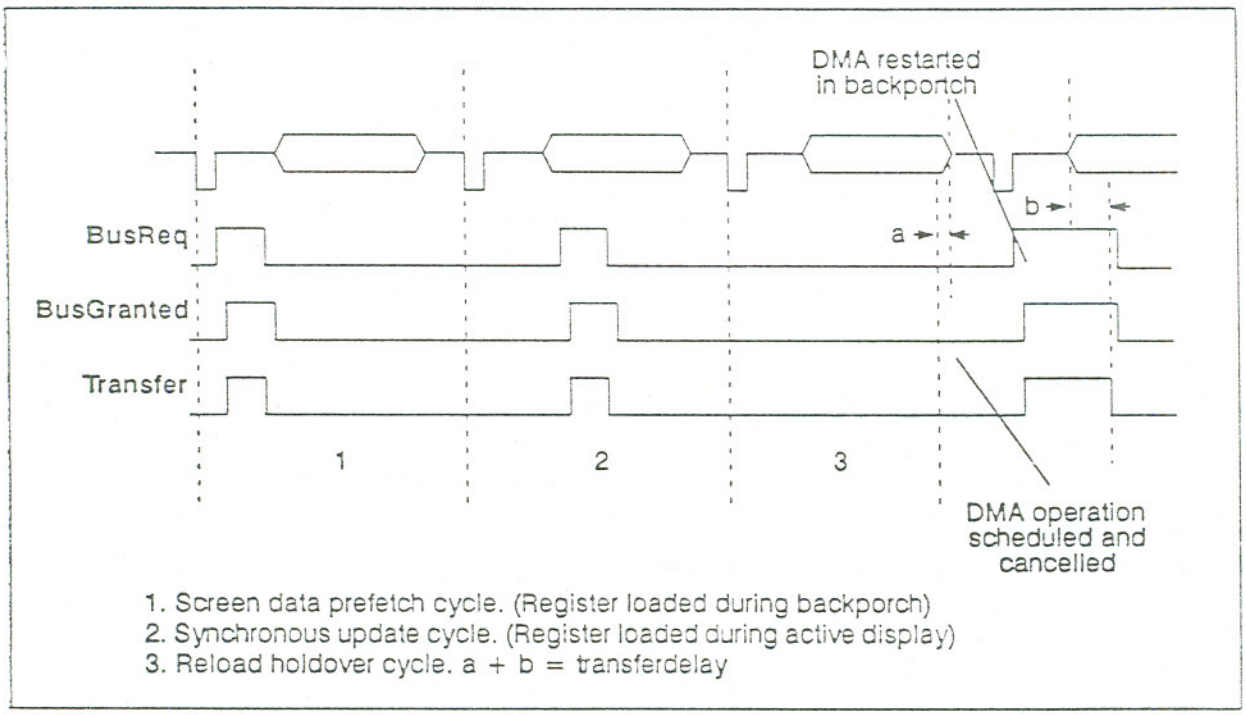

Figure 1.20 Data transfer operational behaviour

Figure 1.19 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G332 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

It should be noted that the G300 signals **notShiftClk**, **notSerialClk** and **Transfer** are all designed to be buffered by inverting buffers outside the G300 and so are the logical inverses of the signals driving the VRAMs.

MemInit defines the number of periods of **notSerialClk** before the G300 asserts **busRequest**. This is the first event which signals the start of a transfer cycle. When the host processor returns **busGranted** the G300 asserts **Transfer** and drives out the new transfer address to be strobed into the VRAMs. Only after a further number of **notSerialClk** cycles equal to TransferDelay, does the G300 remove **Transfer** (synchronously with respect to **notShiftClk**) and so perform the actual transfer. **busRequest** is also taken away at this point to return the **ADBus** back to the host. The user should arrange for TransferDelay to be sufficiently long to

allow for the worst case bus request latency plus the time required to strobe RAS and CAS with the address supplied from the G300.

The most memory-efficient way of using the transfer cycle feature is to make Meminit + TransferDelay equal to the length of the video RAM shift registers thus packing the bitmap into the smallest possible space, but it is obviously possible to specify a smaller number and then use the remainder of the bitmap as a larger 'world' which can be panned through by modifying the SAM start address between frames.

1.12.9 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

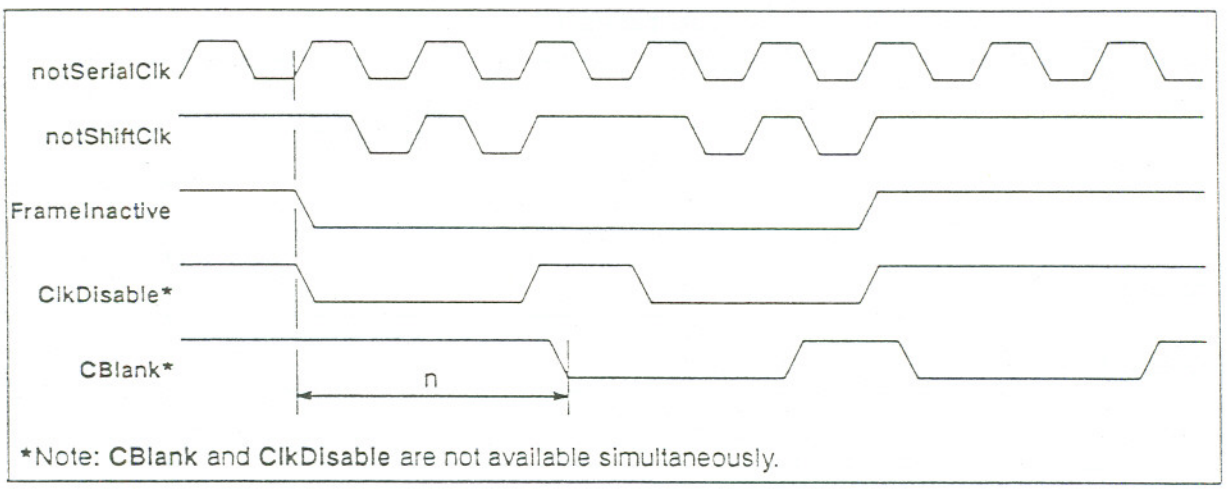

Figure 1.21 Relationship between **notShiftClk**, **FrameInactive**, **CBlank** and **ClkDisable**

FrameInactive goes low on the rising edge of **notSerialClk** immediately prior to the first falling edge of **notShiftClk** of each frame. It goes high on the rising edge of **notSerialClk** immediately after the last falling edge of **notShiftClk** of each frame.

Assuming the G300 is in 8 bits per pixel mode, **ClkDisable** goes low on the rising edge of **notSerialClk** immediately prior to the first falling edge of **notShiftClk** of each line. It goes high on the rising edge of **notSerialClk** immediately after the last falling edge of **notShiftClk** of each line. In all other bit per pixel modes **ClkDisable** is produced as though it were in 8 bit per pixel mode.

CBlank is similar to **ClkDisable** except that it is delayed with respect to **FrameInactive** by n cycles of **notSerialClk** where:

$$n = (2.25 - \text{Control bit 8} + 4 \times \text{Control bit 11} + 2 \times \text{Control bit 10} + \text{Control bit 9})$$

and, in interlace mode, the falling edge of **CBlank** on the first line of each even field is delayed by a further m cycles of **notSerialClk** where:

$$m = \text{linetime}/2 - (\textbf{CBlank} + 2 \times \textbf{HalfSync})$$

..13 The pixel port

1.13.1 Pixel port operation

The pixel port takes in pixel data from the video RAM and has two modes of operation;

mode 1 — pseudo colour, multiplexed input.
mode 2 — gamma corrected full colour, direct input.

The mode is defined by a single bit in the G300 control register. The clock source is set by a combination of wiring option and boot location bit, (See the section on the programming interface). By varying these options it is possible to use the G300 in one of three configurations as shown in table 1.17.

Mode	Clock Option	Video Clock Source	Pixel Route
1	PLL (nom 5MHz)	Output of on-chip PLL	Through LUT
1	Direct (video rate)	ClkIn	Through LUT
2	Direct (video rate)	ClkIn	Through gamma table

Table 1.17 Clock and pixel port options

1.13.2 Mode 1 operation

In mode 1, 8 bits per pixel the G300 latches four 8-bit pixels on **PixDataA0-7**, **PixDataB0-7**, **PixDataC0-7** and **PixDataD0-7** on a single falling edge of **notShiftClk**. These four pixels are then serialised to the full pixel rate internally and applied to the colour palette address inputs in turn — A, B, C and D. In other bit per pixel modes the multiplex ratio is modified automatically.

The eight bit pixels used in mode 1, allow a choice of 256 simultaneous colours from a palette of 16 million. Changing the palette through the programming interface allows rapid colour selection and modification. The colour palette may be loaded and read back via the programming interface (see the G300 memory map). If the G300 memory interface is being used in word-mode, then a colour word may be loaded in one G300 external memory interface cycle and a complete colour palette may be block moved into or out of the G300 by the processor.

Mode 1 allows the pixel input to be multiplexed up to 32 into 1, this allows clocking of the video RAMs well below pixel clock frequency. The G300 supplies a signal **notShiftClk** which is designed to be buffered through a single inverting driver outside the G300 directly into the SC (serial clock) of each of the video ..AMs. This clock pulses once for each new group of pixels required by the display. It is not free running, but stops during line and frame flyback. A free-running clock **notSerialClk** is also generated by the G300. This provides a continous clock synchronous to the video stream. If this clock is loaded identically to **notShiftClk** then its edges will be coincident to **notShiftClk**, it will not stop during flyback, and is always 1/4 pixel frequency. The frequency of **notShiftClk** depends on dot rate and the selected pixel depth.

notSerialClk = dot frequency/4
notShiftClk = dot frequency x bits per pixel/32

By taking a minimum of 4 pixels into the G300 in one go, the clock rate to the video rams for a nominal 110MHz system can be reduced to 27.5 MHz maximum. It is therefore possible to use standard video RAMs without extra multiplexing on the board. It is also possible to drive the pixel data down a backplane using easily available TTL parts in order to gang up extra boards in a distributed system. It has the further advantage that all external clocks and signals are running at comparatively low frequencies.

A memory mapped mask register is available for masking the incoming pixel address to the LUT in mode 1. The contents of this register (mapped onto **ADBus0-7**) are logically ANDed with the incoming pixel stream.

By altering the contents of this register the microprocessor may achieve simple rapid colour changes on the screen.

Colour programming in 1, 2 and 4 bits per pixel modes

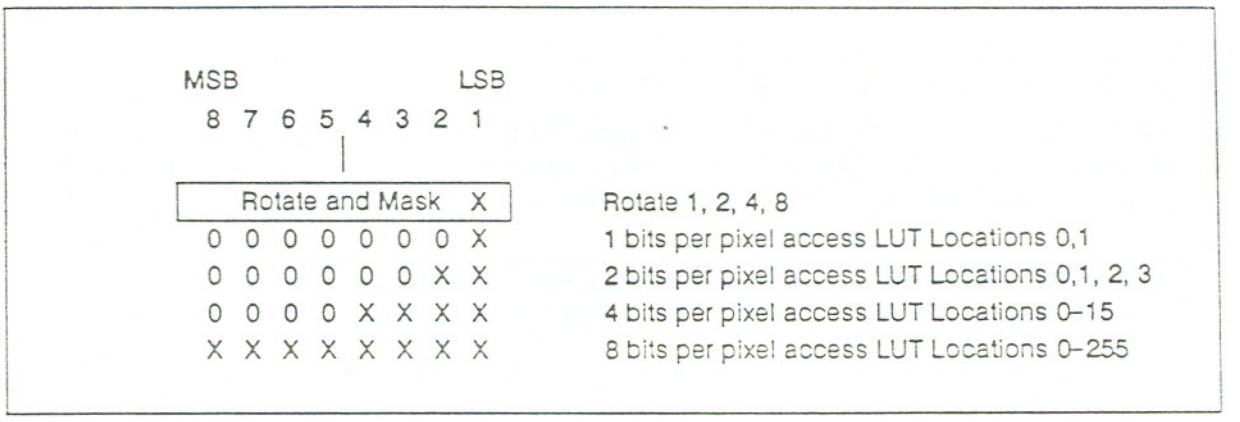

Figure 1.22 Colour palette programming information in 1, 2 and 4 bits per pixel modes

In 1, 2 and 4 bit per pixel modes, each byte is rotated and masked by an extra masking function as shown in figure 1.22

The bits per pixel mode must not be changed while the video timing generator is active.

Pixel ordering

The pixel order is always 'little-endian'. Thus:

In 8 bits per pixel mode, the first pixel displayed is byte A.

In 4 bits per pixel mode, the lower nibble of byte A is displayed first.

In 2 bits per pixel mode, bits 1, 0 of byte A are displayed first.

In 1 bit per pixel mode, bit 0 of byte A is displayed first.

Register Bit 18	Register Bit 17	Bits per pixel
0	0	1
0	1	2
1	0	4
1	1	8

Table 1.18 Programming of bits 17 and 18 of the pixel mode control register

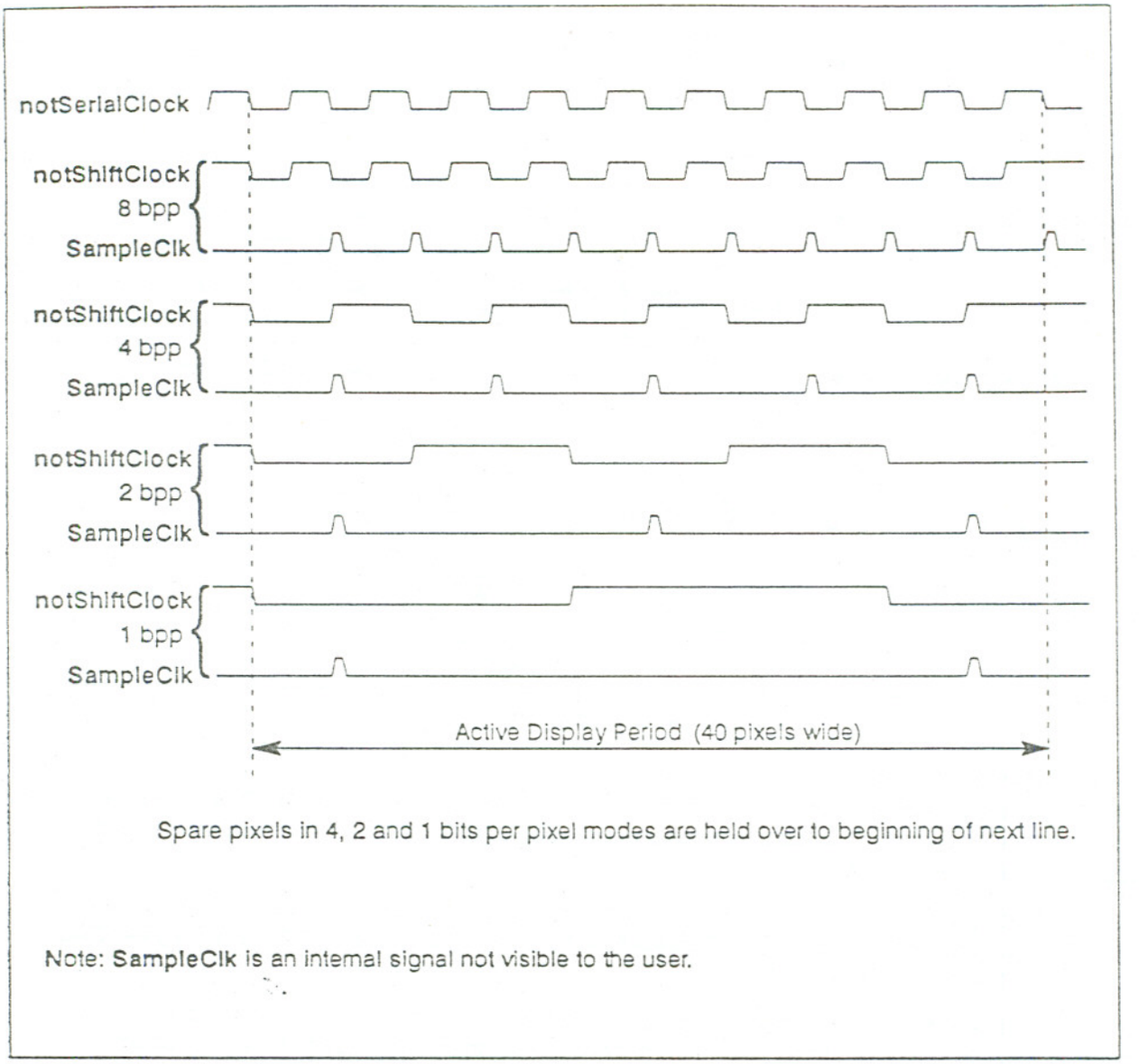

Figure 1.23 Relationship between Serial and Shift Clocks to pixel data in various bits per pixel modes

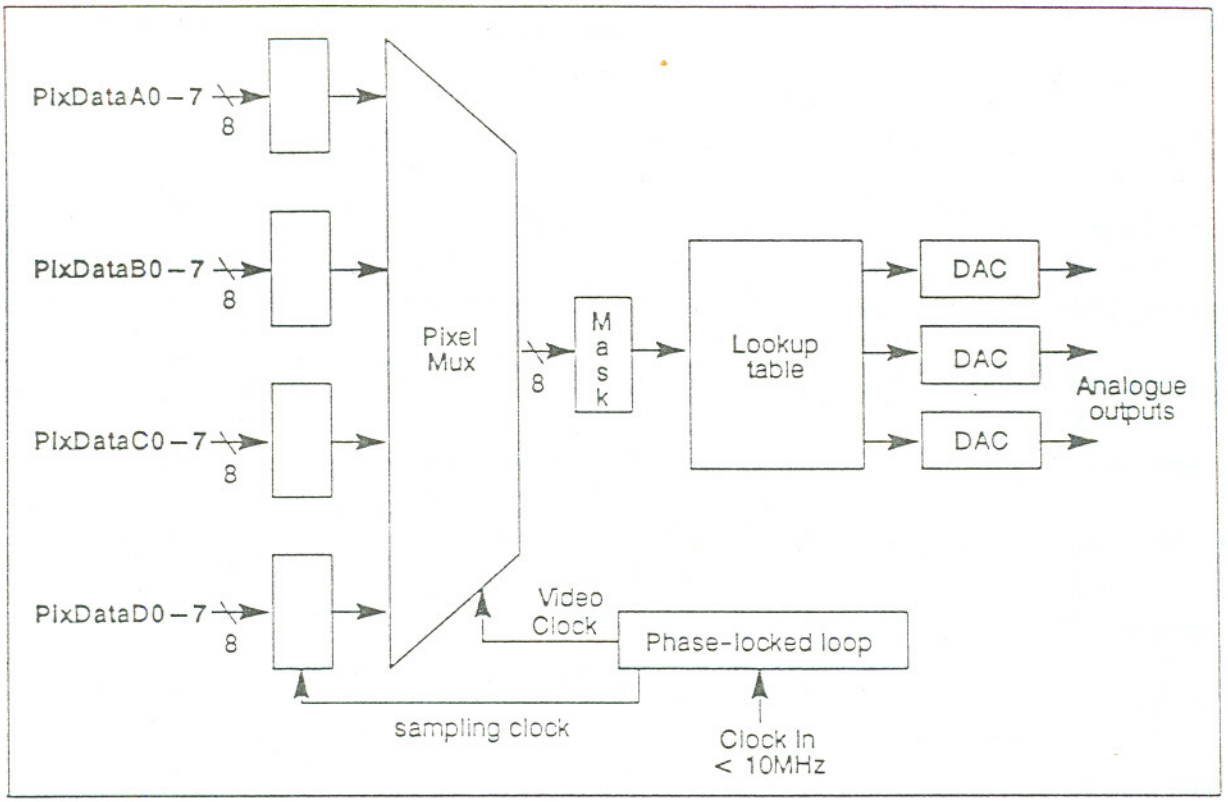

Figure 1.24 Pixel port in mode 1

1.13.3 Mode 2 operation

In mode 2, direct write, pixel inputs are used as three 8-bit addresses into the triple LUT. This allows the use of the full range of up to 16 million colours simultaneously displayed on the screen but requires pixels to be supplied to the G300 at the full video rate.

One 24-bit wide pixel is latched into the G300 on every *rising* edge of the externally supplied pixel clock – **ClkIn**. (The PLL is not used in mode 2.) **PixDataA0-7** feeds the red DAC, **PixDataB0-7** feeds the green DAC and **PixDataC0-7** feeds the blue DAC.

Note that in mode 2, the specified timings for the pixel setup and hold times must be observed, even during flyback, otherwise corruption of the lookup table can occur. Also, the mask register content has no effect on pixel data in mode 2.

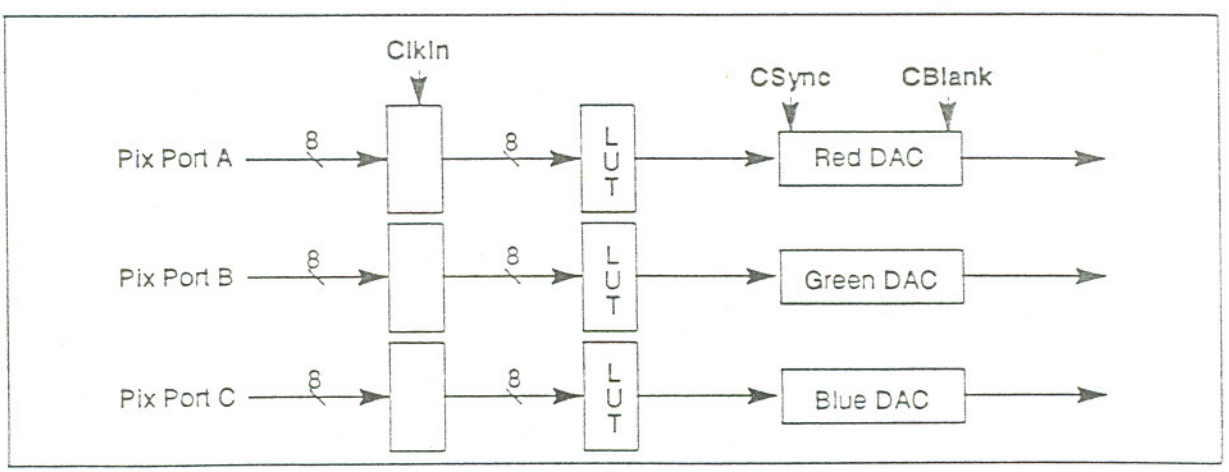

Figure 1.25 Pixel port in mode 2

1.14 The video DACs

1.14.1 General

The video DACs on the G300 have 8-bit resolution at the full video rate. They are designed to drive a doubly terminated 75Ω transmission line and produce analogue video signals compatible with either the RS-170 or RS-343 video standards.

1.14.2 DAC output waveform

The DACs work by sourcing a current proportional to their digital input. The unit current sourced for each digital increment is defined by a reference current drawn from the part using an external current source.

The complete analogue video signal comprises three components as shown in figure 1.26. The current sourced by each component is defined in terms of DACunits. The value of 1 DACunit is set by the reference current drawn from the Iref pin:

$$1\ \text{DACunit} = \text{Iref}/120$$

The colour information output by each gun ranges from 0 to 255 units under control of the digital input from the colour palette or the pixel port.

A black-level pedestal of 20 DACunits is provided. This extra pedestal distinguishes between a displayed value of intensity 0 during display (ie black) and the 'blacker than black' level present when the electron beam is blanked for flyback. When enabled (by setting the relevant bit in the control register), this extra level is switched on only during the active display time of each line. It is switched off during blanking so as to ensure no visible trace of the beam appears on the screen during this period.

A sync pedestal, again selected using the control register, is provided to allow the superposition of the sync timing signals on the video outputs. When this composite sync option is selected the sync level is added to the output during blanking and active display. Sync pulses are present on all three of the video DACs. The size of the sync pedestal is 108 DAC units.

Table 1.19 defines the value of each of the three components which make up the complete video output current sourced by each DAC.

	Colour Data (Full Scale)	Black Level Pedestal	Sync
units	255	20	108

Table 1.19 DAC output level components

Both the black-level pedestal and the sync signals may be independently turned on or off by setting bits 12 and 3 in the control register respectively.

(Note that the extra blanking pedestal units, if used, add to the full scale deflection so that the current source must be redefined in order to use this mode).

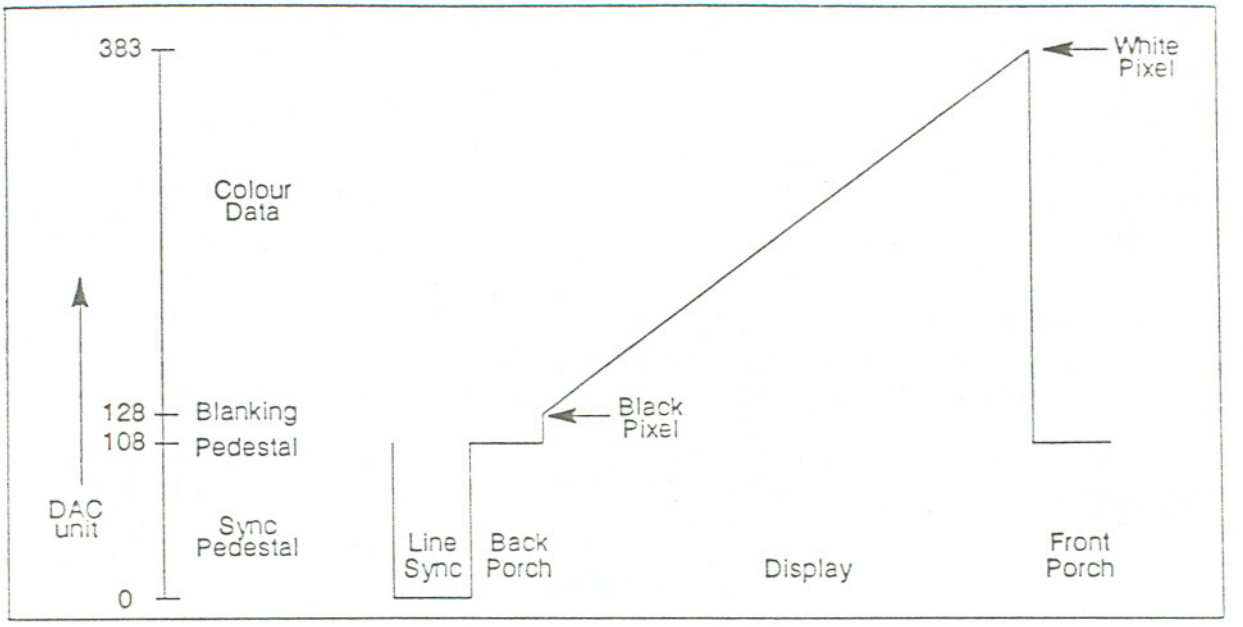

Figure 1.26 DAC output levels

1.14.3 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution		8		bits	
VO(max)	Output voltage			1.5	V	2
IO(max)	Output current			32	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5
	Glitch Energy		75		pVSec	2, 6, 7
IREF	Reference current	7		10	mA	
VREF	Reference voltage	VDD −3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **Ground** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω + 30 pF with IREF = −8.88mA.

7 This parameter is sampled not 100% tested.

Symbol	Parameter	-66 Max.	-85 Max.	-100 Max.	-110 Max.	Units	Notes
	DAC Risetime	6	6	4	4	ns	1
	DAC Settling time	15.3	11.7	10	9.1	ns	1, 2, 3
Note: These figures are not characterised and are subject to change							

Notes

1 Load = 37.5Ω + 30pF, IREF = −8.88mA.

2 From a 2% change in output voltage until settling to within 2% of the final value.

3 This parameter is sampled not 100% tested.

1.14.4 Power supply and current reference

It is recommended that a high frequency decoupling capacitor (preferably a chip capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between AVdd and Ground to provide the best possible supply to the analogue circuitry of the DACs.

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 1.27 shows four designs of current reference.

Figure 1.27(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 1.27(a)–(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuits 1.27(b) and 1.27(c) the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 1.27(c)).

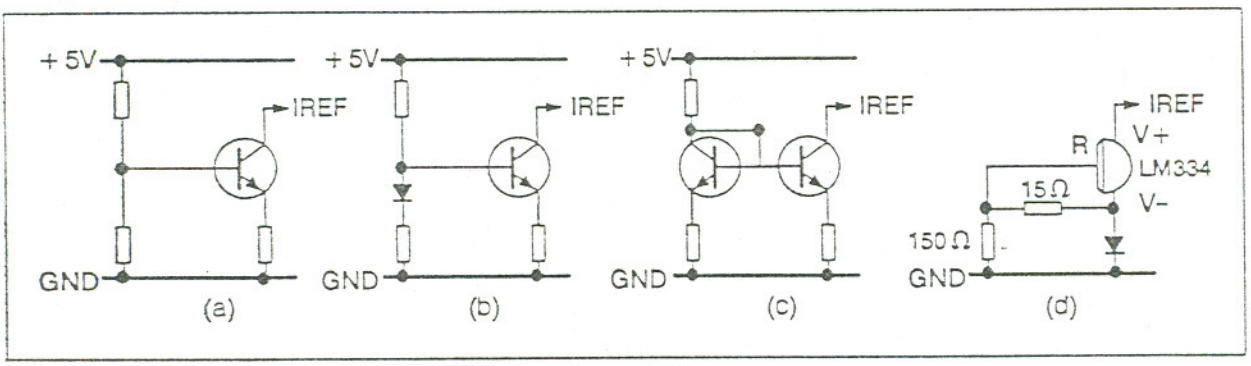

Figure 1.27

1.14.5 Current reference – decoupling

The DACs in the IMS G300 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VDD. This will enable the current reference to track both low and high frequency variations in the supply.

1.14.6 Analogue output – line driving

The G300 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 1.28. The effective load seen by the G300 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G300 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G300 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and will not cause a degradation of the image quality.

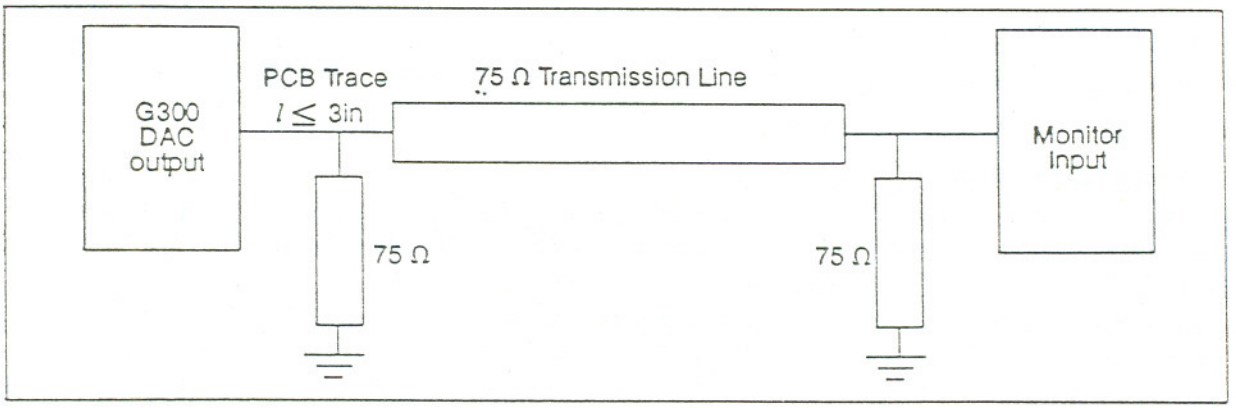

Figure 1.28 DAC output loading

1.14.7 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G300 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G300 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

1.15 Clock generation and phase locked loop

1.15.1 Introduction

The IMS G300 has two alternate clocking schemes which between them provide a high degree of system flexibility. The primary clocking system uses a phase locked loop on the chip to multiply the low frequency (< 10MHz) input clock up to the required video data rate. This scheme is used only when the part is in mode 1 and contributes to its overall ease of design. A full dot-rate clock is supplied to the **ClkIn** pad for the alternate scheme, which must be used when the IMS G300 is in mode 2 and when mode 1 is to be driven in 'times one' configuration.

1.15.2 ClkIn

When the PLL is to be used, **ClkIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **ClkIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits. Phase locked loop mode is selected by placing a capacitor between **CapPlus** and **CapMinus**, and then writing a 'one' to the boot location bit 5.

1.15.3 CapPlus, CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1μF capacitor to be connected between **CapPlus** and **CapMinus**. A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm. The connections must not touch power supplies or other noise sources.

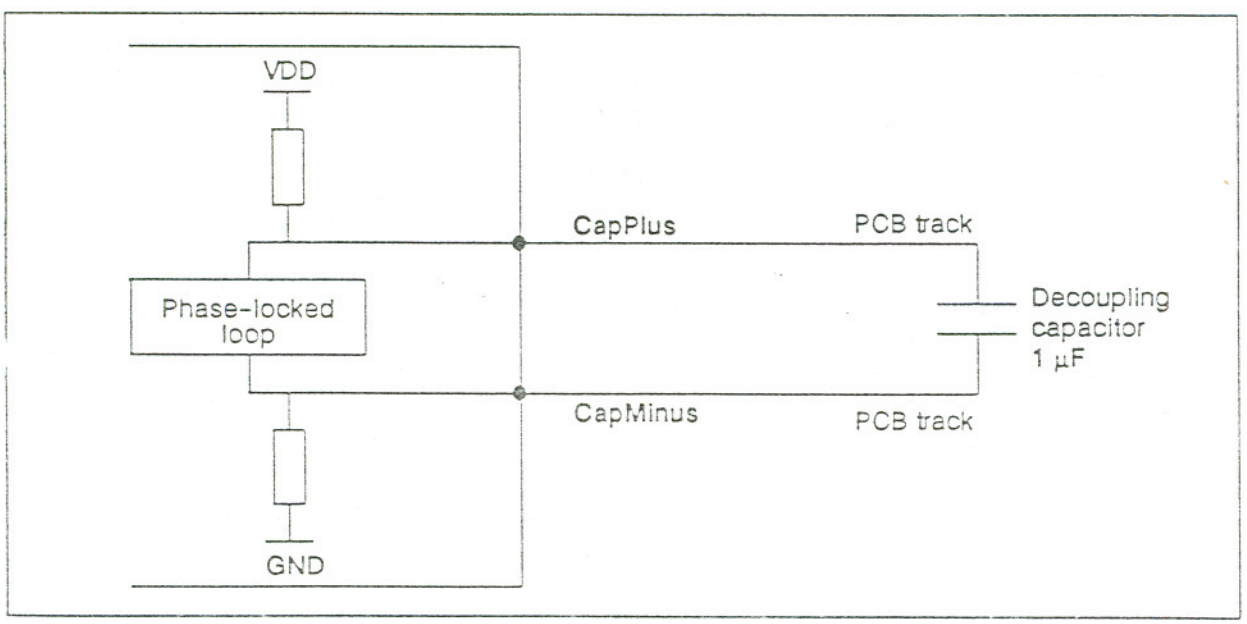

Figure 1.29 Recommended PLL decoupling

1.15.4 Speed selection

The multiplication factor of the phase locked loop is set by writing a binary value to the IMS G300 boot location. This location is enabled for writing by performing a reset cycle. Once it has been written to, another reset must be performed before reprogramming is possible. Only **ADBus**[5:0] are valid as data during these write cycles, in all other respects they conform to the diagrams given in section 1.12. Although all possible multiplication factors will work with all permissible input frequencies up to the speed rating of the

part, the quoted figures are guaranteed only if the recommended combinations are adhered to. The multiplication factor selected is the binary number written to the boot location bits[4:0].

1.15.5 Recommended input clock and multiplication factors

Intermediate video data frequencies can be produced by choosing the multiplication factor for the quoted frequency closest to that desired and varying the input clock frequency to achieve the correct value. Clock multiplication factors less than 5 are not allowed.

It is possible to produce the full range of frequencies from a 5 MHz input clock (in steps of 5 MHz) but the PLL will be more susceptible to power supply noise and clock input jitter when a very high multiplication factor is used.

Parameter	Min.	Max.
Input frequency	5MHz	10MHz
Multiplication factor	5	31*

*Subject to speed rating of device.

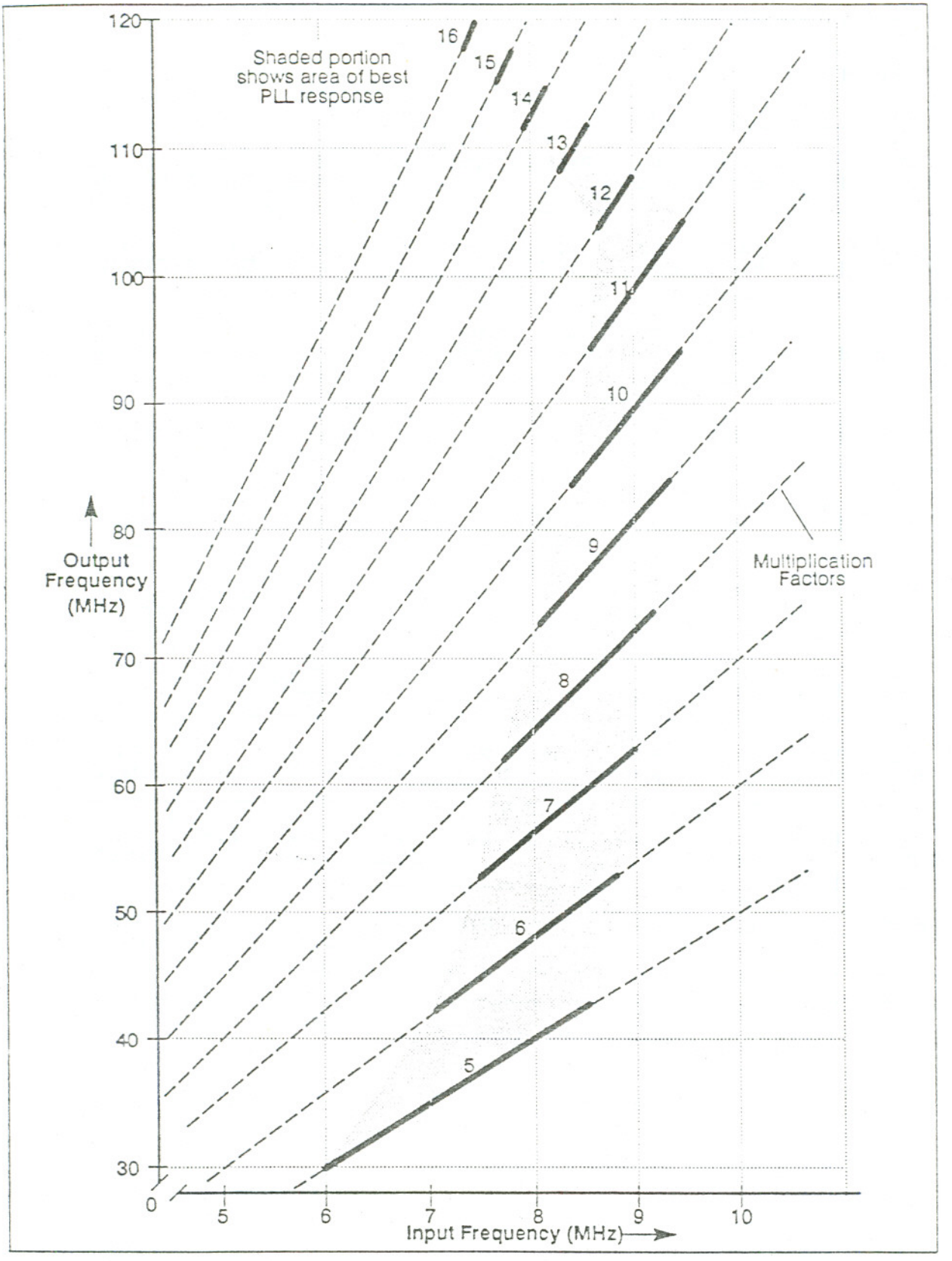

Figure 1.30 Best multiplier settings for G300 PLL

1.16 Package specifications

1.16.1 84 pin grid array package

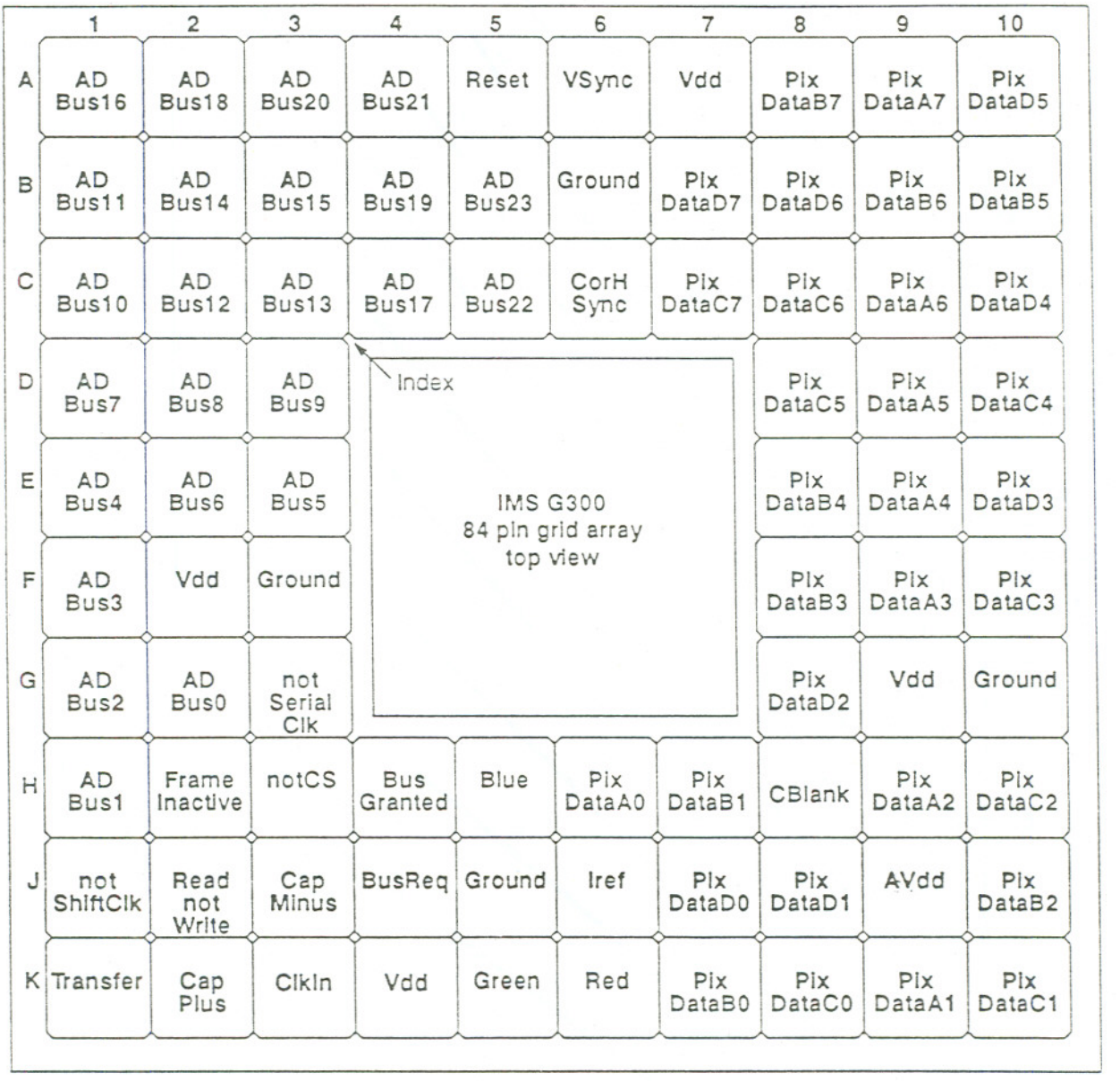

Figure 1.31 IMS G300 pin configuration

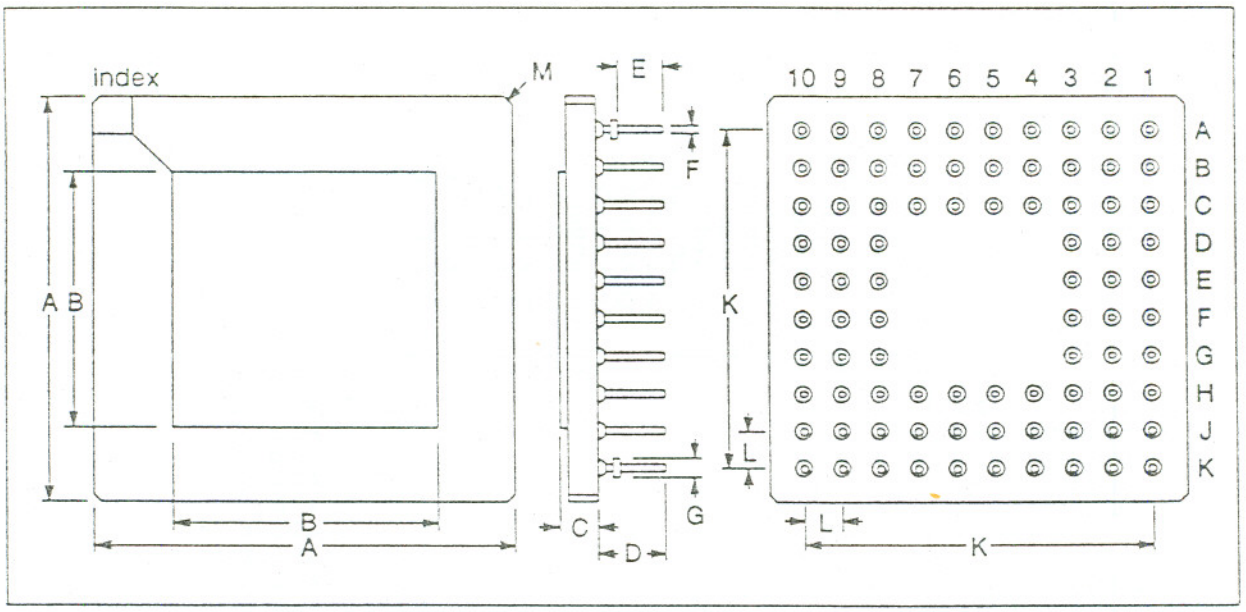

Figure 1.32 84 pin grid array package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	26.924	±0.254	1.060	±0.010	
B	17.019	±0.127	0.670	±0.005	
C	2.456	±0.278	0.097	±0.011	
D	4.572	±0.127	0.180	±0.005	
E	3.302	±0.127	0.130	±0.005	
F	0.457	±0.025	0.018	±0.001	Pin diameter
G	1.143	±0.127	0.045	±0.005	Flange diameter
K	22.860	±0.127	0.900	±0.005	
L	2.540	±0.127	0.100	±0.005	
M	0.508		0.020		Chamfer
Package weight is approximately 7.2 grams					

Table 1.20 84 pin grid array package dimensions

1.16.2 100 lead quad cerpack package

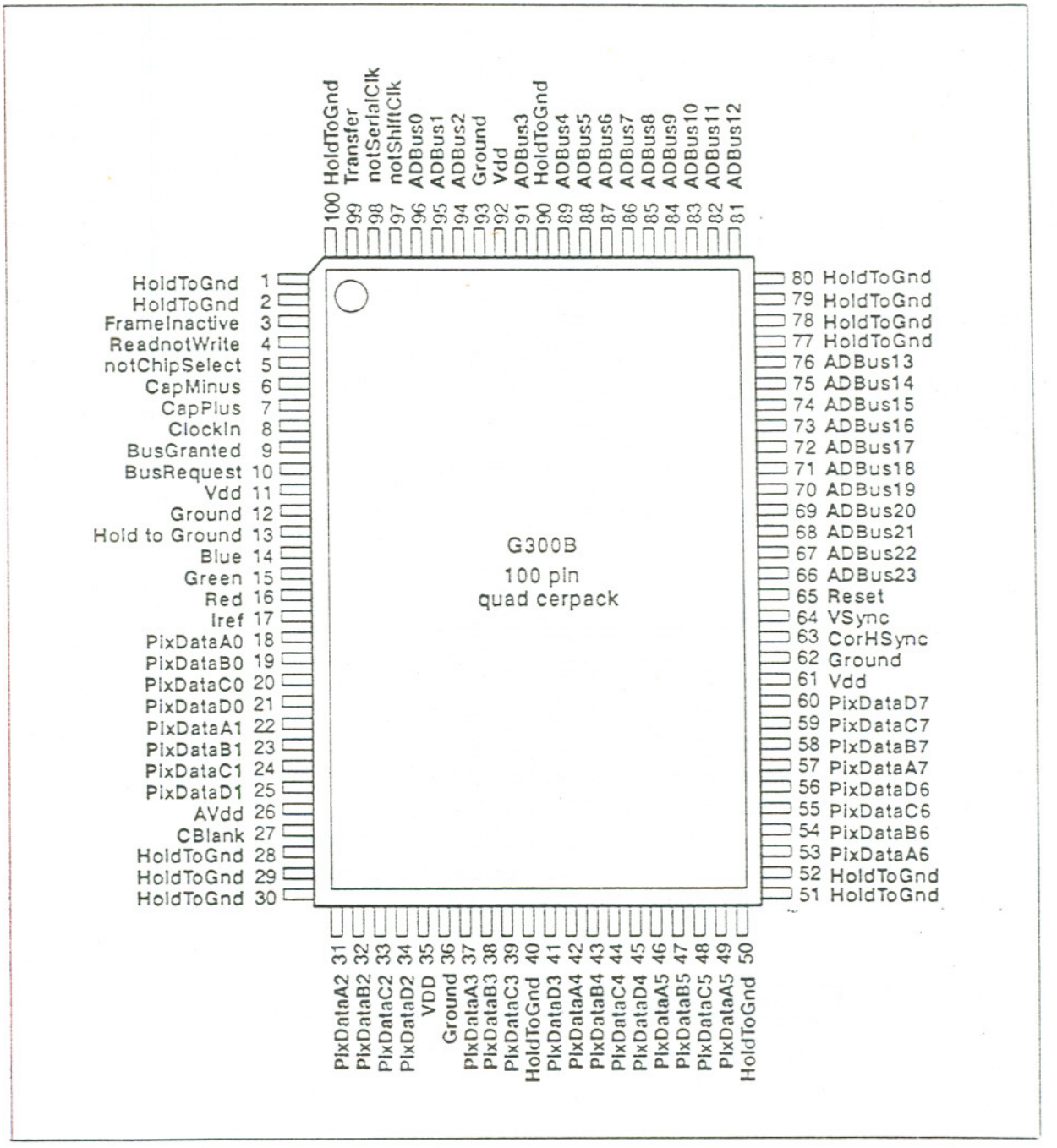

Figure 1.33 IMS G300 pin configuration

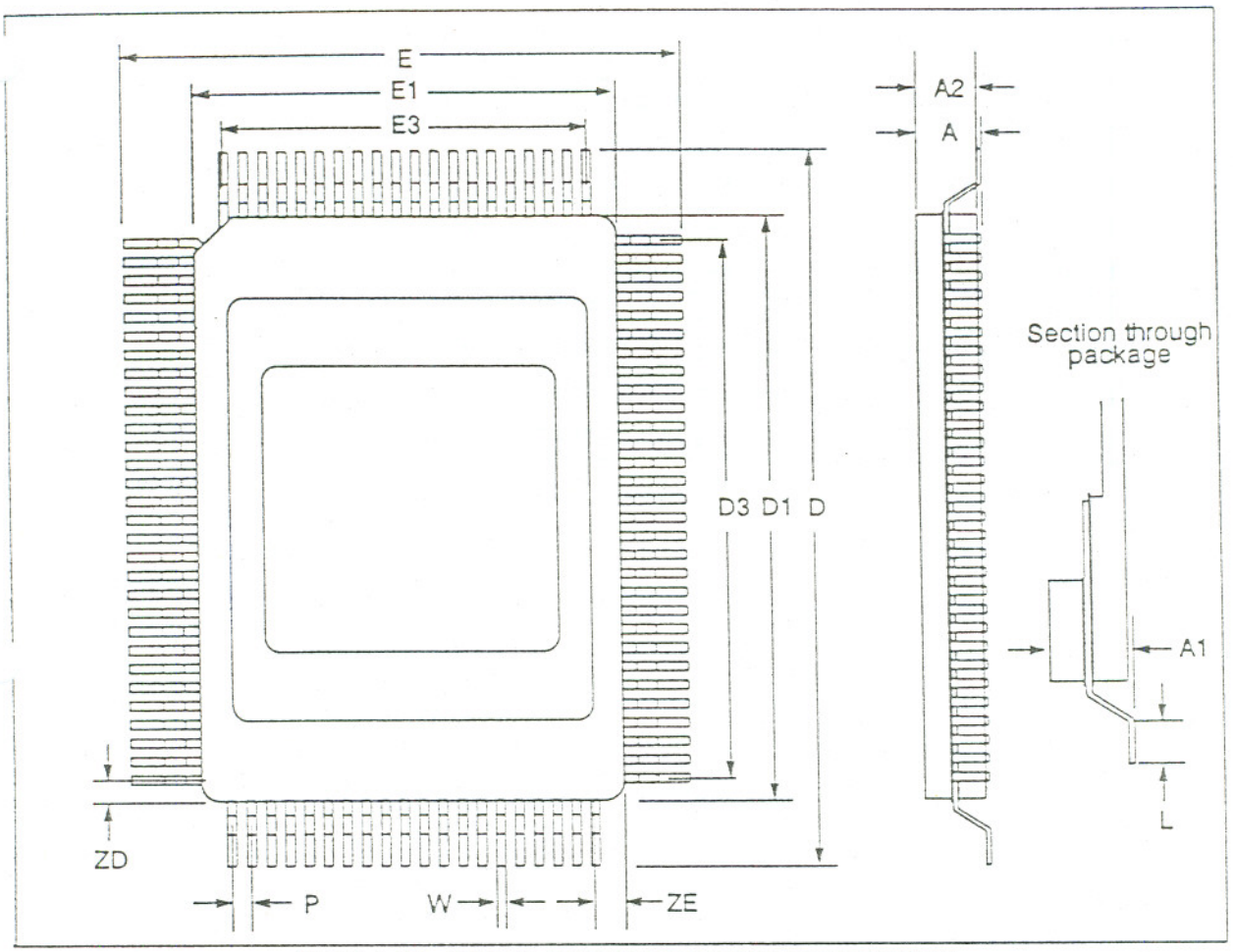

Figure 1.34 100 pin quad cerpack package dimensions

Dim	Millimetres			Inches			Notes
	Min	Nom	Max	Min	Nom	Max	
A			3.300			0.130	
A1	0.000		0.250	0.000		0.010	
A2	2.550	2.800	3.050	0.100	0.110	0.120	
D	23.650	23.900	24.150	0.931	0.941	0.951	
D1	19.900	20.000	20.100	0.783	0.787	0.791	
D3		18.850			0.742		Ref.
ZD		0.580			0.023		Ref.
E	17.650	17.900	18.150	0.695	0.705	0.715	
E1	13.900	14.000	14.100	0.547	0.551	0.555	
E3		12.350			0.486		Ref.
ZE		0.830			0.033		Ref.
L	0.650	0.800	0.950	0.026	0.031	0.037	
P		0.650			0.026		BSC
W	0.220		0.380	0.087		0.015	

Table 1.21 100 lead quad cerpack package dimensions

1.16.3 Ordering information

Device	Clock rate	Package	Part number
IMS G300	66 MHz	84 pin PGA	IMS G300G-66
IMS G300	85 MHz	84 pin PGA	IMS G300G-85
IMS G300	100 MHz	84 pin PGA	IMS G300G-10
IMS G300	110 MHz	84 pin PGA	IMS G300G-11
IMS G300	66 MHz	100 pin QUAD CERPAC	IMS G300F-66
IMS G300	85 MHz	100 pin QUAD CERPAC	IMS G300F-85
IMS G300	100 MHz	100 pin QUAD CERPAC	IMS G300F-10
IMS G300	110 MHz	100 pin QUAD CERPAC	IMS G300F-11

1.17 Programming example for Hitachi HM-4219/4119 monitor

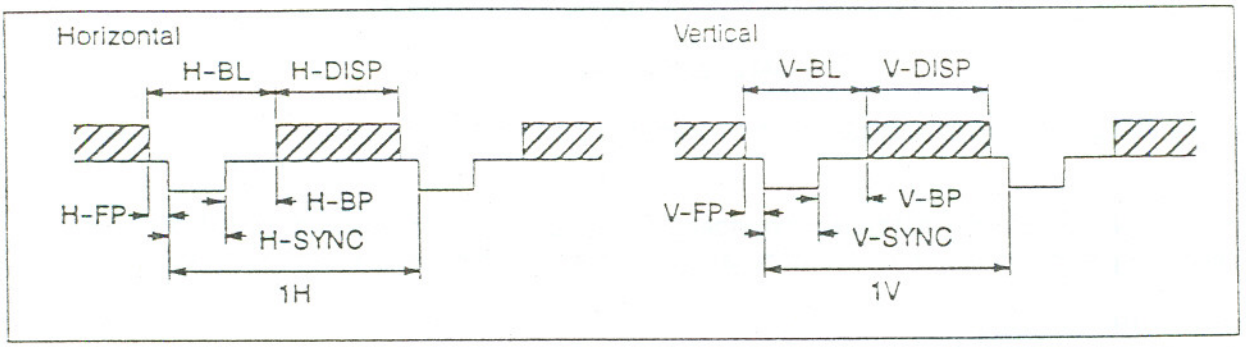

Figure 1.35 Hitachi HM-42/4119 timing

	Item	Equation	Rating (64kHz Version)	Unit
a	Resolution H		1280	Pixel
b	Resolution V		1024	Pixel
c	Pixel rate		9.296	ns
d	Pixel frequency	1 / c	107.573	MHz
e	H-DISP	a x c	11.899	µs
f	H-BL	g + h + i	3.800	µs
g	H-FP		0.200	µs
h	H-SYNC		1.600	µs
i	H-BP		2.000	µs
j	1H		15.699	µs
k	H frequency	1 / j	63.7	kHz
l	V-DISP	b x j	(1024H)	ms
m	V-BL*	n + o + p	(37H)	ms
n	V-FP		(0H)	ms
o	V-SYNC		(3H)	ms
p	V-BP*		(34H)	ms
q	1V	l + m	(1601H)	ms
r	V frequency	1 / q	60.0	Hz

Table 1.22 Recommended timings for monitor (64kHz version)

* Note: These parameters do not map directly to CVC register values.

1.17.1 Calculation of parameters

At the recommended pixel rate of 9.296ns,

screen unit = 4 x 9.296ns = 37.184ns

All line timing parameters are calculated as multiples of this figure.

Line Scan period

$$\text{Linetime} = 15.699\mu s / 37.184ns = 422.19$$

$$\text{so set Linetime} = 422$$

This obeys the rule associated with the Linetime parameter; that it should be an even number of screen units.

If it is absolutely necessary to meet the recommended linescan frequency then it is best to specify the input clock frequency as the variable but, in practice, all monitors will synchronise to a close approximation.

Line sync pulse

The G300 constructs this from two halfsync periods so:

$$\text{Halfsync} = 1.6\mu s / (2 \times 37.184ns) = 21.5$$
$$\text{so set Halfsync} = 21 \text{ screen units}$$

Backporch

$$\text{Backporch} = 2\mu s / 37.184ns = 53.7$$
$$\text{so set Backporch} = 54 \text{ screen units}$$

Display

This parameter is set in terms of the number of pixels you wish to display so in this case:

$$\text{Display} = 1280 / 4 = 320 \text{ screen units.}$$

Frontporch

There is no explicit frontporch parameter; this period being implied as the difference between the sum of the other parameters and the linetime period.

$$\begin{aligned}\text{Frontporch} &= \text{Linetime} - ((\text{Halfsync} \times 2) + \text{Backporch} + \text{Display}) \\ &= 422 - (21 \times 2 + 54 + 320) \\ &= 6 \text{ screen units} \\ &= 6 \times 37.184 \text{ ns} = 0.223 \mu s\end{aligned}$$

Which compares with the monitor requirement of 0.2 μs.

The 'halfline point' rule is obeyed by these timings since:

$$(\text{HalfSync} \times 2) + \text{Backporch} + \text{Display} < \text{Linetime} / 2 > (\text{HalfSync} \times 2) + \text{Backporch}$$

In a non interlaced system such as this the remaining two line parameters are actually used only during frame flyback in order to count in multiples of half a line time. In an interlaced system, the parameter Short-display is used to construct the short displayed lines at top and bottom of the screen if the total number of displayed lines is odd. BroadPulse is used to produce the low pulses in a tesselated frame sync period. Both of these parameters must always be programmed whether or not your system explicitly uses them.

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ShortDisplay

$$\begin{aligned} \text{Shortdisplay} &= (\text{Linetime} / 2) - [(\text{HalfSync} \times 2) + \text{Backporch} + \text{Frontporch}] \\ &= 211 - (42 + 54 + 6) \\ &= 109 \text{ screen units} \end{aligned}$$

$$\begin{aligned} \text{BroadPulse} &= (\text{Linetime} / 2) - \text{Frontporch} \\ &= 211 - 6 \\ &= 205 \text{ screen units} \end{aligned}$$

Frame timing parameters

All frame timings are specified in terms of half line times.

Number of Displayed lines is 1024

$$\text{VDisplay} = 1024 \times 2 = 2048$$

Which complies with the requirement that each frame must contain an even number of half lines.

The G300 produces frame flyback waveforms in accordance with the broadcast standards which means that:

$$\text{VSync} = \text{PreEqualisation} = \text{PostEqualisation}$$
$$\text{VSync} = 6$$

Total Blanked period is 37H so :

$$\text{VBlank} = 74 - (6 \times 3) = 56$$

Which is a whole number of lines.

HalfSync	=	21
BackPorch	=	54
Display	=	320
LineTime	=	422
ShortDisplay	=	109
BroadPulse	=	205
VSync	=	6
VBlank	=	56
VDisplay	=	2048

The remaining three parameters are concerned with management of the video RAM bitmap. Assuming that 256K video RAMs are being used, the shift register length will be 256 bits. The sum of the parameters MemInit and TransferDelay must not exceed this figure unless some external form of multiplexing is used which generates an effective register length greater than this. It is possible to use parameters which total less than 256 in order to implement a hardware pan function, but for the purpose of this example, we will assume that all of the bitmap is to be displayed. Thus:

$$\text{Meminit} + \text{TransferDelay} = 256$$