CHAPTER 7

Format Examples

7.1 Introduction

This module supplies a flexible software interface between the Floppy Disk Drive(s) and the SCSI bus. This gives a large range of media formats which can be supported.

A separate document called "Floppy Disk Format Examples" will give example drive tables for general media formats.

Use these tables as they are or change them according to your needs.

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CHAPTER 8

Hardware Interface

8.1 Features

- 6809 microprocessor
- 6844 direct memory controller
- 2 MHz operating frequency
- 64 kBytes of RAM/EPROM on board memory space
- floppy disk drive controller
- SCSI bus controller (target/initiator)

8.2 General Description

The CC93 is a high-performance floppy disk drive interface based on the 6809 microprocessor. Data transfer to and from the floppy disk controller and SCSI bus controller may be programmed to occur under DMA control. All devices can interrupt the processor. The board is capable of supporting a total of 64 kByte RAM and EPROM. The amount of EPROM is not restricted. The I/O map can be placed anywhere in the memory-map and takes only 256 bytes of memory. The floppy disk controller can handle all currently known types of floppy disk drives e.g.:

8" (DS/DD)
5.25" mini
3.50" micro
and 5.25" eight inch compatible.

Mixing of different types of drives is possible. The SCSI bus controller can be used in target mode as well as in initiator mode. In initiator mode other devices may be accessed like e.g. hard disks, tape streamers, other computers etc.. In target mode the single board computer acts as an intelligent interface to the floppy disk drives.

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CHAPTER 9

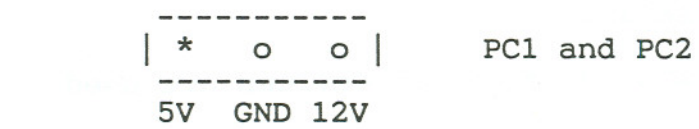
Installation Instructions

9.1 Introduction

This chapter provides the hardware preparation and installation instructions for the CC93 module.

9.2 Power Connection

Power for the electronics of the board is derived from the P1 and P2 connectors from the VMEbus. Power to the drives can be taken from the PC1 and PC2 connectors:



If the total supply current at +12Vdc to the drives does not exceed at any time the maximum current rating for the VMEbus +12Vdc power pin of P1 (about 1.5 Amp at 60 degrees C), then it is not necessary to use the extra pins on the P2 connector.
If power does exceed this maximum current (for instance, a hard disk drive at power on), the extra power pins of P2 must be connected externally to the power supply of the VMEbus.

9.3 Jumper Settings

All jumper settings discussed in the next section are illustrated as seen from the component side with the P1 connector downwards. Pin number one is identified as '*', rest of pins are identified as 'o'.

9.3.1 JB1: Eprom Size Select

This jumper selects what size of Eprom devices are used.

8 kbyte Eprom

32 kbyte Eprom

9.3.2 JB2: Ram Size Select

This jumper selects what size of Ram devices are used.

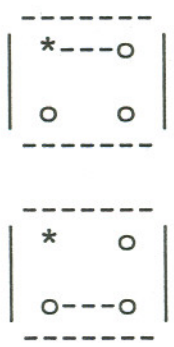
8 kbyte Ram

32 kbyte Ram

9.3.3 Socket 1

This socket may only contain Ram devices. Jumper blocks JB2 and JB3 must be set according to the size of Ram devices used.

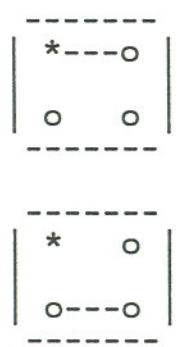
JB3: Ram size select



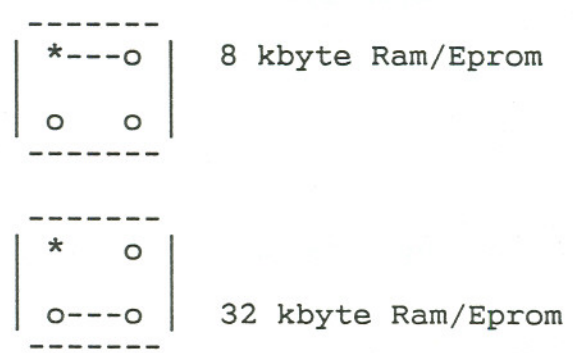
9.3.4 Socket 2

This socket may contain Ram or Eprom type of devices. A Ram device must be of the same size as used in Socket 1. An Eprom device must be of the same size as used in Socket 3.

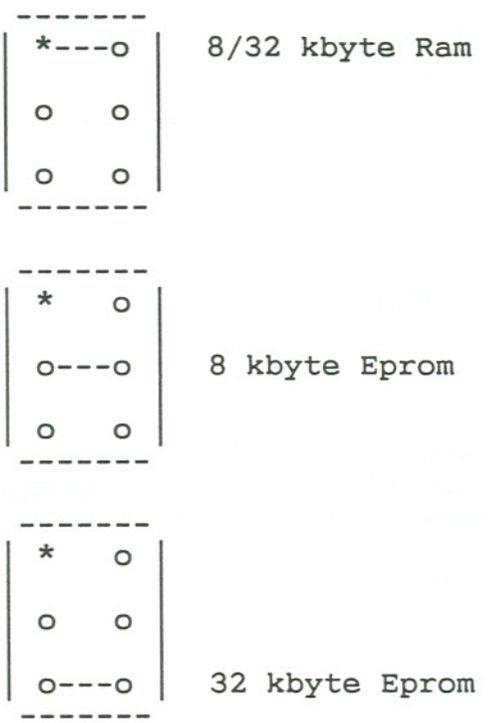
JB4: Ram/Eprom size select



JB5: Ram/Eprom size select



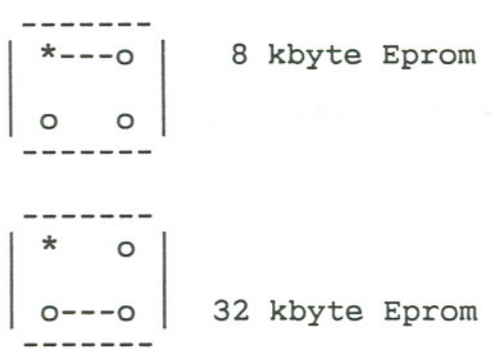
JB6: Ram/Eprom size select



9.3.5 Socket 3

This socket may only contain Eprom devices. Jumper blocks JB1 and JB7 must be set according to the size of Eprom devices used.

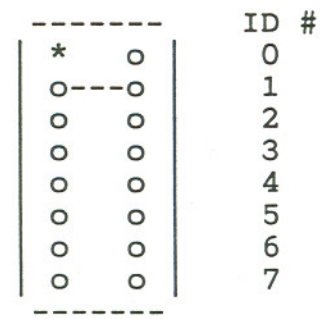
JB7: Eprom size select



9.3.6 JB8: SCSI ID Number

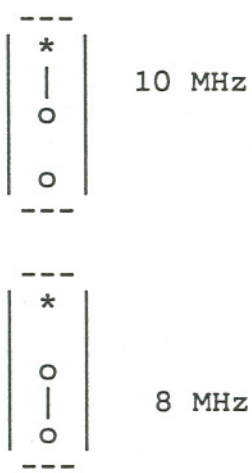
Before connecting the board to a SCSIbus an ID number must be selected. Only one jumper may be installed.

JB8



9.3.7 JB9: Clock Select

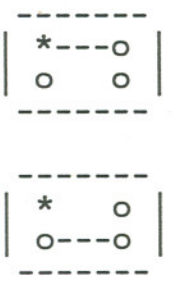
This jumper selects between an 8 or a 10 MHz clock to the NCR5386.



9.3.8 JB11: SCSI Parity Enable

This jumper enables and disables the parity check of the SCSI controller. The controller will however always generate odd parity on all SCSI bus transfers regardless the setting of this jumper. The setting of the jumper is sampled only once when the board is reset. Only one jumper may be installed.

JB11



Parity disabled

Parity enabled

9.3.9 JB12: Termination Power

When this jumper is removed, the termination power (TRMPWR) for the resistor networks must be supplied via the SCSI bus. When the jumper is installed the resistor networks use the +5V of the board and TRMPWR will be fed to the SCSI bus (using a diode).

9.3.10 JB13/14: Hard Disk ID

The pins of these jumper blocks are one to one connected and allow easy ID change while the Hard Disk drive is mounted.

9.4 Connector Assignments

PIN ASSIGNMENTS P3/P4
3.50" Floppy disk drive connector

P3/P4	name
2	drive type select
4	head load
6	select 4
8	index
10	select 1
12	select 2
14	select 3
16	motor on
18	direction
20	step
22	write data
24	write enable
26	track 0
28	write protect
30	read data
32	side select
34	ready

note:
all odd pins are connected to ground.

PIN ASSIGNMENTS P2 and P5/P6
SCSI bus connector

P2A	P5/P6	name
1	2	-DB(0)
2	4	-DB(1)
3	6	-DB(2)
4	8	-DB(3)
5	10	-DB(4)
6	12	-DB(5)
7	14	-DB(6)
8	16	-DB(7)
9	18	-DB(P)
10	20	GND
11	22	GND
12	24	GND
13	26	TRMPWR
14	28	GND
15	30	GND
16	32	-ATN
17	34	GND
18	36	-BSY
19	38	-ACK
20	40	-RST
21	42	-MSG
22	44	-SEL
23	46	-C/D
24	48	-REQ
25	50	-I/O

note:
pins 1 to 25 of P2C are connected to ground except pin 13,
odd pins of P5/P6 are connected to ground except pin 25.

CHAPTER 10

Theory of Operation

10.1 Introduction

This chapter provides a description of the CC93 floppy interface module. A block diagram is given in appendix A. With the aid of the schematic diagram in appendix B an explanation of the operation is given.

10.2 Central Processor Unit

The implemented microprocessor (U28) is of the type MC68B09.

The chip is supplied with an 8 MHz clock derived from the 16 MHz oscillator (U24) by means of the 74393 counter (U33). The CPU generates two phase shifted 2 MHz clock signals E and Q. All timing of the on board address and databus is related to those two signals.

Inputs to the processor:

/IRQ: is connected to a "wired-or" DMA, Floppy and SCSI interrupt signal

/DMA-BREQ and /HALT are connected to the DMA controller (U29); see appropriate section.

All on board peripherals (except the DMA controller) do not use the Motorola type of bus protocol and an adjustment is made to the R/W generation. Further discussions on this topic are found in the next section.

10.3 Direct Memory Access Controller

The implemented direct memory access controller (U29) is of the type MC68B44.

The controller must be initialized for a DMA transfer by the processor. The data transfer may be either from a peripheral to RAM or from RAM to a peripheral. The controller will take no actions until a peripheral requests a DMA transfer. A peripheral signals the controller that data transfer is wanted by asserting the proper TxRQ (transmit request) line.

The controller then asserts the /DMA-BREQ or /HALT line to the processor to gain control of the bus. The CPU will assert DGRNT (DMA grant) when the bus is available. The controller addresses

the proper RAM location and asserts the TxAK (transmit acknowledge) line to the peripheral which asked for service. The data will be transferred directly between the peripheral and RAM.

The bus is released by the DMA controller after the transfer has taken place and normal CPU operation will continue.

Peripherals serviced by the DMA controller are the Floppy disk drive controller and the SCSI bus controller.

Both the 6809 and the 6844 use R/W to determine the direction of data transfer and use the select line to the peripheral and the E clock to strobe the data transfer. All the other controller circuits use an other type of protocol. They expect two signals apart from the select line: /RD (read peripheral) and /WR (write peripheral). Transfer direction and timing are combined in these signals. The Pal16L8 (U4) is programmed to generate these signals using the R/W line and E and Q clocks. During DMA transfer reading from a peripheral has to be combined with writing to RAM and writing to a peripheral with reading from RAM. To accomplish this an exchange is made to the /RD and /WR signals when in DMA mode (programmed within the Pal16L8 (U4)).

10.4 Memory and I/O Selection

The memory map consists of three blocks; an EPROM block, a RAM block and an I/O block. Decoding is done on 256 Byte boundaries. The EPROM area is located at the top of the memory map.

There are three sockets (U25-U27) available in which either 8k or 32k RAM or EPROM memory devices may be inserted. Three sockets are provided to make it possible to locate the EPROM lower boundary on any 256 byte boundary without loosing the unused Eprom area for RAM.

The location of the I/O block is independent of the location of the RAM and EPROM blocks and may be configured anywhere in the map. The total occupied area for I/O is only 256 bytes of memory.

Location of the I/O block and the EPROM lower boundary is programmed within the FPLA (U5). See appropriate section.

Eight select signals are generated in the decoder (U1). Five are used for selecting:

- the SCSI bus controller (U16)
- the Floppy disk controller (U30)
- the DMA controller (U29)
- the Local Control Register (U12-U13)
- the Floppy disk controller terminal Count pin (U30)

The remaining select lines are not used.

Each select signal decodes a 32 byte area in the I/O map.

10.5 Floppy Disk Interface

The CC93 uses the 16 Mhz clock oscillator circuit (U24) as the base for the signals for writing and formatting sectors. The clock frequency applied to the floppy disk controller (U30) is 8 MHz in 8 inch mode and 4 MHz in 5.25 inch mode. The incoming data from the floppy disk drive is converted by a WD9216/01 data separator (U31) in two separate signals: RDW (read data window) and RDD (read data) . The 16 MHz clock is divided into 8, 4, 2, 1 MHz and 500, 250 kHz signals (U33). These signals are supplied to the Pal16L8 (U34) which generates the correct write clock dependent on the density and drive type.

The write data from the floppy disk controller is clocked into an eight bit serial in parallel out shift register (U32) in order to generate the proper preshift delays. The delay time depends on the signals P0, P1 and MFM from the controller (U30) and the drive mode from the Local control register (U12-U13).

The processor must write command bytes into the FDC. After receiving the last command byte, the FDC starts executing the command. Data may be transferred under control of the DMA controller.

10.6 SCSI Bus Interface

The interface uses the SCSI bus controller chip NCR5386 (U16). A correct functioning of the interface as defined by the ANSI X3T9.2 committee is thereby guaranteed. For details concerning the programming of the chip see the NCR5386 SCSI Protocol Controller Data Sheet.

A jumperblock (JB 8) must be used for the selection of an ID number.

10.7 Local Control Register

An eight bit latch is used as a control register for several purposes.

The meaning of the used bits are respectively:

Bit 0	selection of drive type 5.25"
Bit 1	turn motor on 5.25" drive
Bit 2	enable the interrupt of floppy interface
Bit 3	read the floppy interface interrupt status
Bit 4	not used
Bit 5	not used
Bit 6	read the SCSI interface interrupt status
Bit 7	SCSI parity enable

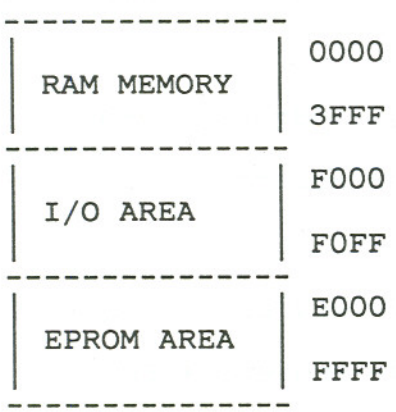
CHAPTER 11

Programming Considerations

11.1 Memory Map

A possible configuration of the memory map is given below.

The memory map is divided in three parts:



RAM	$0000 - $3FFF	16 kBytes
I/O	$F000 - $F0FF	256 Bytes
EPROM	$E000 - $FFFF	8 kBytes - 256 Bytes (I/O)

Using the lower boundary of the I/O map as the baseaddress, the peripherals are located as follows:

	offset
SCSI control 16 registers	base address + $00
Floppy control 2 registers	base address + $20
DMA control 22 registers	base address + $40
not used	base address + $60
Local Contr. R. 1 register	base address + $80
not used	base address + $A0
Terminal Count Floppy Contr.	base address + $C0
not used	base address + $E0

Both the location of the I/O block and the EPROM and RAM boundaries may be changed to accommodate personal needs. See APPENDIX E for details on this subject.

Use I/O baseaddress + I/O base offset as a base address for addressing the registers in the peripherals.

11.2 DMA Controller

The 6844 is capable of supporting up to four different peripherals (channels).

The assignment of the channels is as follows:

channel 0	SCSI bus controller
channel 1	Floppy disk controller
channel 2	not used
channel 3	not used

Three modes of data transfer are programmable in the 6844:

Mode 1 and Mode 2 are single byte transfers;

Mode 1: uses the cycle steal mode by asserting the /DMA-BREQ line to the processor

Mode 2: uses the halt steal mode by asserting the /HALT line to the processor

Mode 3 is a burst transfer mode which uses the halt steal mode by asserting the /HALT line to the processor.

The interrupt output is "wired-or" connected to the /IRQ input of the CPU.

The 22 registers of the 6844 are addressed at I/O baseaddress + $40 + register address

For programming the 6844 see Motorola 8 Bit Microprocessors Data Manual.

11.3 Floppy Disk Controller

The uPD765 is capable of controlling up to four floppy disk drives.

Normally all four drives should be of the same type (8" or 5.25") due to the fact that both types use different data transfer rates. By controlling the clock frequency to the FDC through a software switch (local control register bit 0) it is made possible to interface to both types without making hardware changes. This bit also controls the level of pin 2 of the 5.25" FDD connector (P4). This provides a means of signalling the FDD to change from 5.25" to 8" mode.

Also it is possible to turn the motor on and off (local control register bit 1).

It is not possible to enable/disable the interrupt output in the uPD765 internally. Therefore a software switch is provided to control the interrupt output enable (local control register bit 2).

It is not possible to determine if the FDC has asserted the interrupt output through reading a single register of the controller. By reading local control register bit 3 the status of the interrupt output is available to the CPU.

When using the FDC in Non-DMA mode the TC pin (Terminal Count) of the FDC must be asserted by the processor. Accessing the I/O memory with an offset of $C0 to $DF will assert the TC pin of the FDC. When using the FDC in DMA mode the DMA Controller will assert the TC pin.

Summery of bits in the local control register used for controlling the FDC.

Bit 0: 0 drive type is 8"
1 drive type is 5.25"
this bit is read/write
used for switching between 8" and 5.25" drives

Bit 1: 0 motor off 5.25" drive
1 motor on 5.25" drive
this bit is read/write
used to turn motor on and off when interfacing to 5.25 " type of drive

Bit 2: 0 interrupts from FDC disabled
1 interrupts from FDC enabled
this bit is read/write
used to prevent the FDC from generating interrupts

Bit 3: 0 interrupt output FDC is not asserted
1 interrupt output FDC is asserted
this bit is read only
used to determine if FDC is source of interrupt

All write bits are reset during system reset

The interrupt output is "wired-or" connected to the /IRQ input of the CPU.

The 2 registers of the uPD765 are addressed at I/O baseaddress + $20 + register address

For programming the uPD765 see NEC Data Sheets.

11.4 SCSI Bus Controller

The NCR5386 operates in both the initiator and the target roles and can therefore be used in host adapter and control unit designs. The device supports arbitration, including reselection.

It is not possible to determine if the SCSI controller has asserted the interrupt output through reading a single register of the controller without loosing some information about the interrupt (see data sheet NCR5386). By reading local control register bit 6 the status of the interrupt output is available to the CPU.

Bit 7 in the local control register can be used to read the parity enable jumper JB11. It can be sampled by the software to determine if parity on the SCSI bus should be checked or not.

Summery of bits in the local control register used for the SCSI bus controller.

Bit 6: 0 interrupt output SCSI controller is not asserted
1 interrupt output SCSI controller is asserted
this bit is read only

used to determine if SCSI bus
controller is source of interrupt

Bit 7: 0 parity should be checked
1 parity should not be checked
this bit is read only
used to determine if parity should
be checked on the SCSI bus

The interrupt output is "wired-or" connected to the /IRQ input of the CPU.

The 16 registers of the NCR5386 are addressed at I/O baseaddress + $00 + register address

For programming the NCR5386 see NCR5386 Protocol Controller Data Sheet.

11.5 Local Control Register

This register is used to control and monitor several functions of the board. A brief description of the use of the different bits is given here; for details see appropriate sections.

The Local Control Register is addressed at I/O baseaddress + $80.

Summery of bits in the local control register used for controlling the FDC.

Bit 0: 0 drive type is 8"
1 drive type is 5.25"
this bit is read/write
used for switching between 8" and 5.25" drives

Bit 1: 0 motor off 5.25" drive
1 motor on 5.25" drive
this bit is read/write
used to turn motor on and off when interfacing to
5.25 " type of drive

Bit 2: 0 interrupts from FDC disabled
1 interrupts from FDC enabled
this bit is read/write
used to prevent the FDC from generating interrupts

Bit 3: 0 interrupt output FDC is not asserted
1 interrupt output FDC is asserted
this bit is read only
used to determine if FDC is source of interrupt

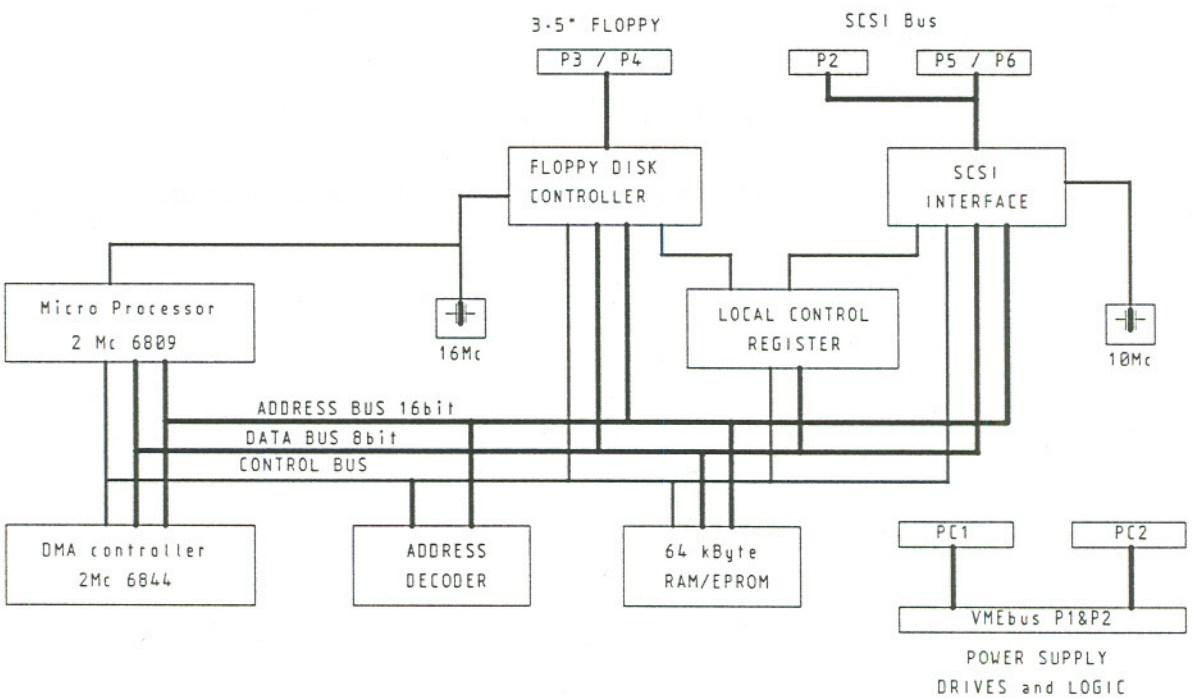
Summery of bits in the local control register used for the SCSI bus controller.

Bit 6: 0 interrupt output SCSI controller is not asserted
1 interrupt output SCSI controller is asserted
this bit is read only
used to determine if SCSI bus
controller is source of interrupt

Bit 7: 0 parity should be checked
1 parity should not be checked
this bit is read only
used to determine if parity should
be checked on the SCSI bus

APPENDIX A

BLOCK DIAGRAM



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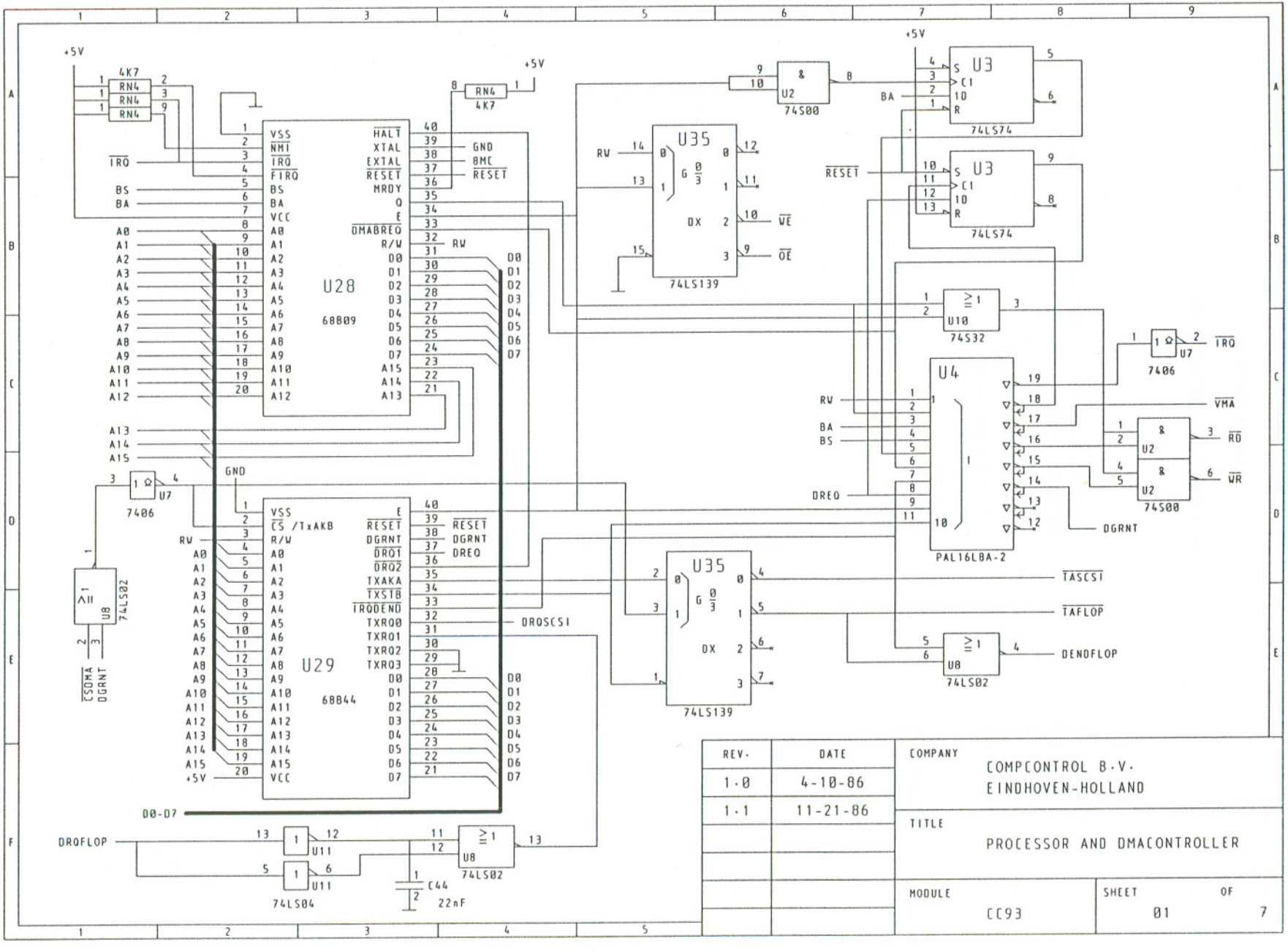
APPENDIX B

SCHEMATIC DIAGRAMS

Sheet 1	Processor and dma controller
Sheet 2	Memory and I/O selection
Sheet 3	Floppy disk controller
Sheet 4	SCSI interface
Sheet 5	FDC connector / Reset circuit / Control register
Sheet 6	VMEbus and SCSIbus connectors
Sheet 7	Power supply decoupling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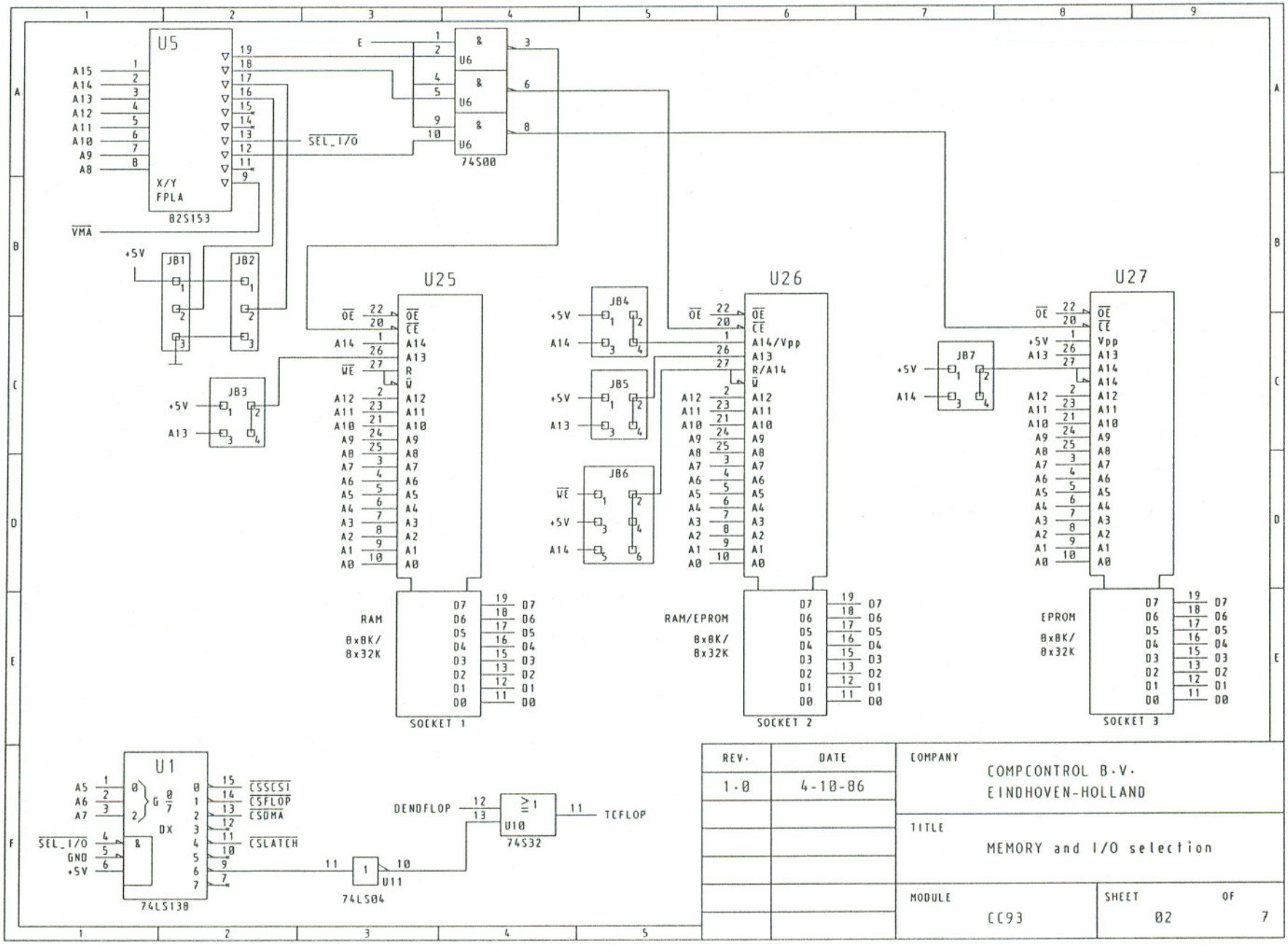
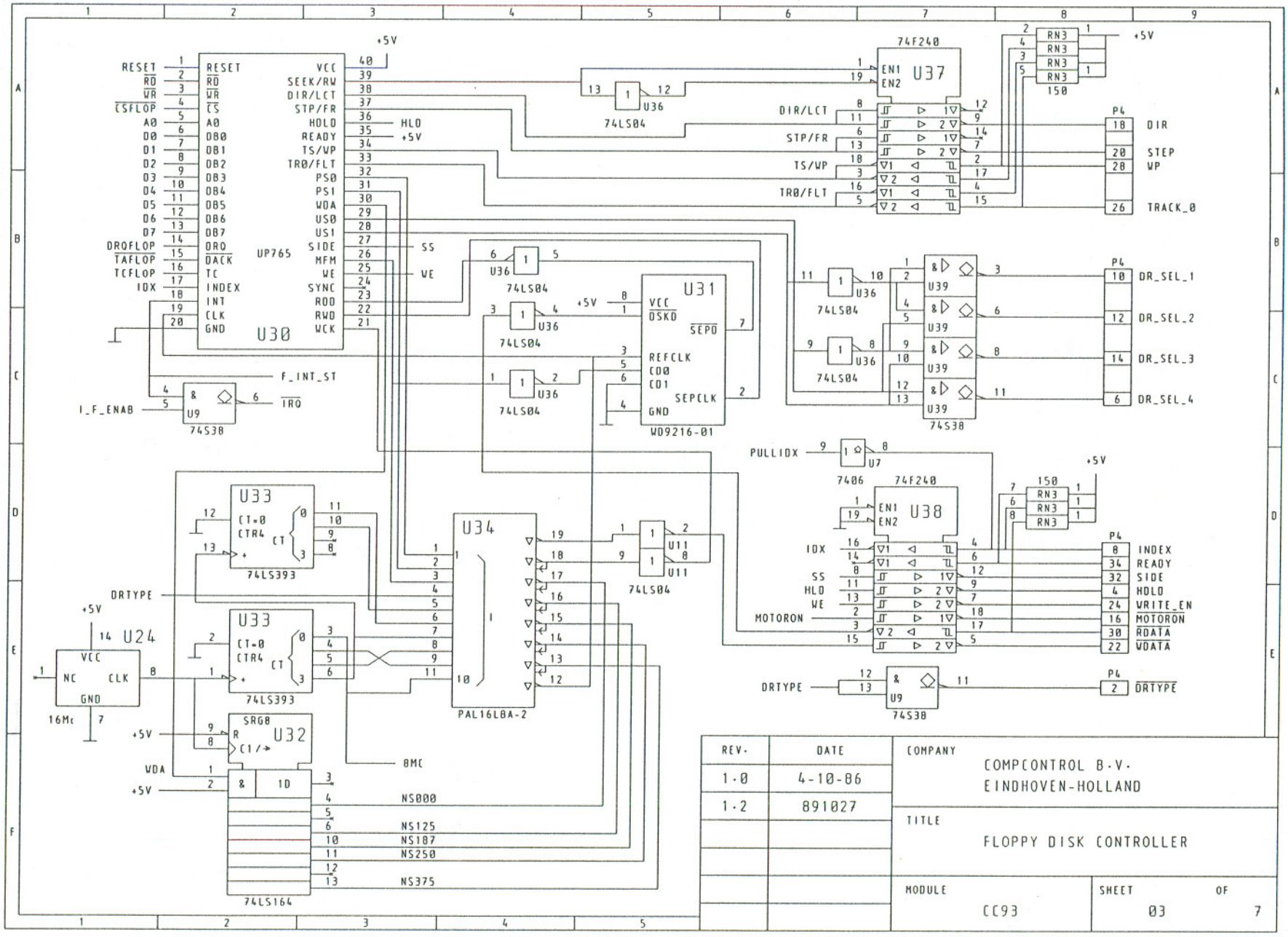
4K7
RN4
U28
68B09
U29
68B44
VSS
NMI
IRQ
FIRQ
BS
BA
VCC
HALT
XTAL
EXTAL
RESET
MRDY
Q
E
DMABREQ
R/W
GND
8MC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
U7
7406
U8
74LS02
CS /TxAKB
DGRNT
DREQ
IRQ1
IRQ2
TXAKA
TXSTB
IRQDEND
TXRQ0
TXRQ1
TXRQ2
TXRQ3
CSDMA
DROSCSI
D0-D7
DROFLOP
U11
74LS04
C44
22nF
U2
74S00
U3
74LS74
U35
74LS139
U10
74S32
U4
PAL16L8A-2
RW
VMA
RD
WR
DGRNT
TASCSI
TAFLOP
DENOFLOP
REV.
DATE
1.0
4-10-86
1.1
11-21-86
COMPANY
COMPCONTROL B.V.
EINDHOVEN-HOLLAND
TITLE
PROCESSOR AND DMACONTROLLER
MODULE
CC93
SHEET
01
OF
7


U5
X/Y FPLA
82S153
A15 A14 A13 A12 A11 A10 A9 A8
VMA
SEL_I/O
E
U6
74S00
+5V
JB1
JB2
JB3
A13
U25
U26
U27
JB4
JB5
JB6
JB7
A14
WE
OE
CE
R/W
A14/Vpp
A13
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
RAM
8x8K/
8x32K
SOCKET 1
RAM/EPROM
SOCKET 2
EPROM
SOCKET 3
U1
A5 A6 A7
DX
GND
CSSCSI
CSFLOP
CSDMA
CSLATCH
74LS138
DENDFLOP
TCFLOP
U10
74S32
U11
74LS04
REV.
1.0
DATE
4-10-86
COMPANY
COMPCONTROL B.V.
EINDHOVEN-HOLLAND
TITLE
MEMORY and I/O selection
MODULE
CC93
SHEET
02
OF
7



REV.	DATE
1.0	4-10-86
1.2	891027

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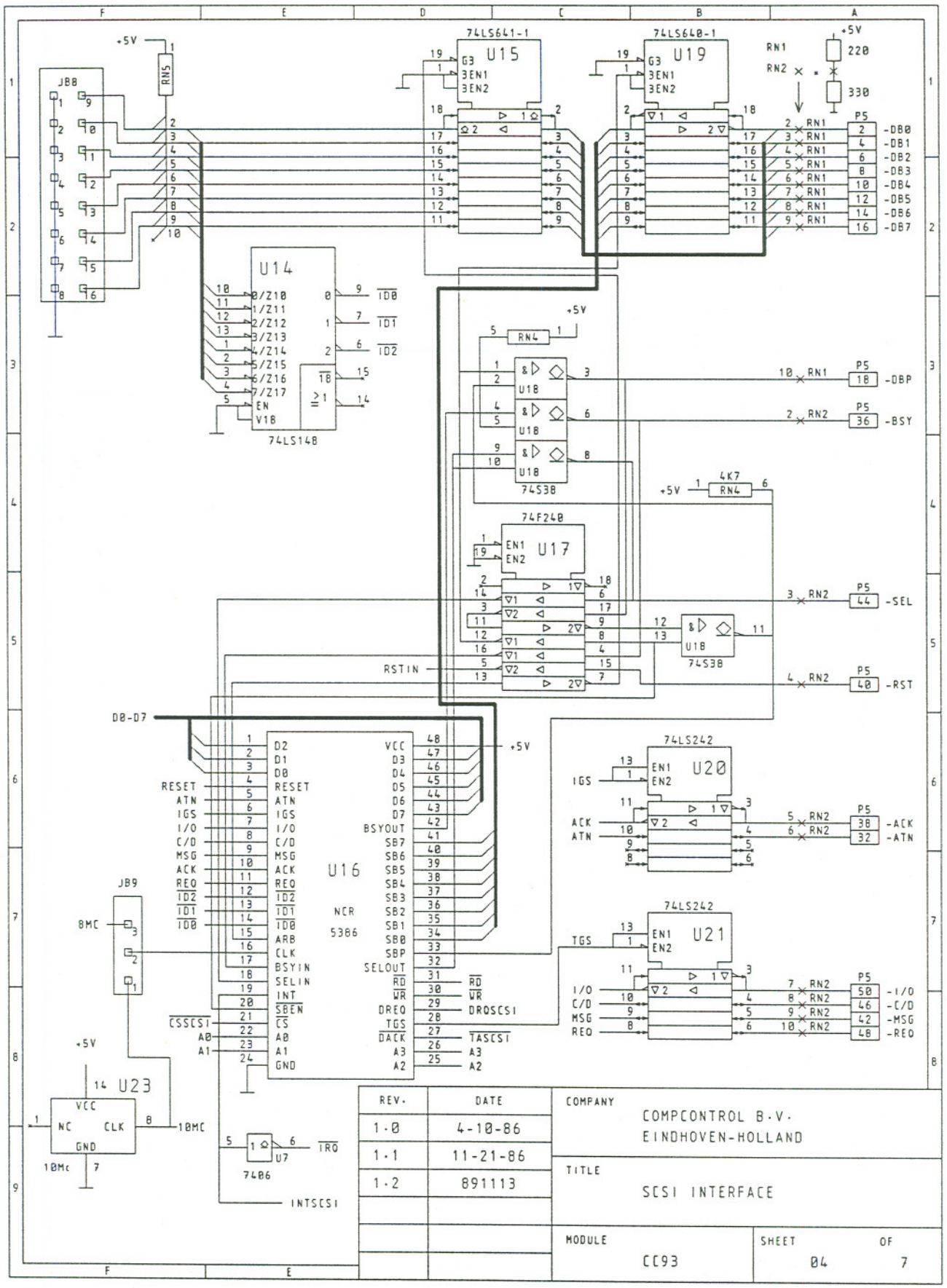
TITLE: FLOPPY DISK CONTROLLER

MODULE: CC93

SHEET: 03 OF 7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U19
+5V
RN1
220
RN2
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JB8
RN5
P5
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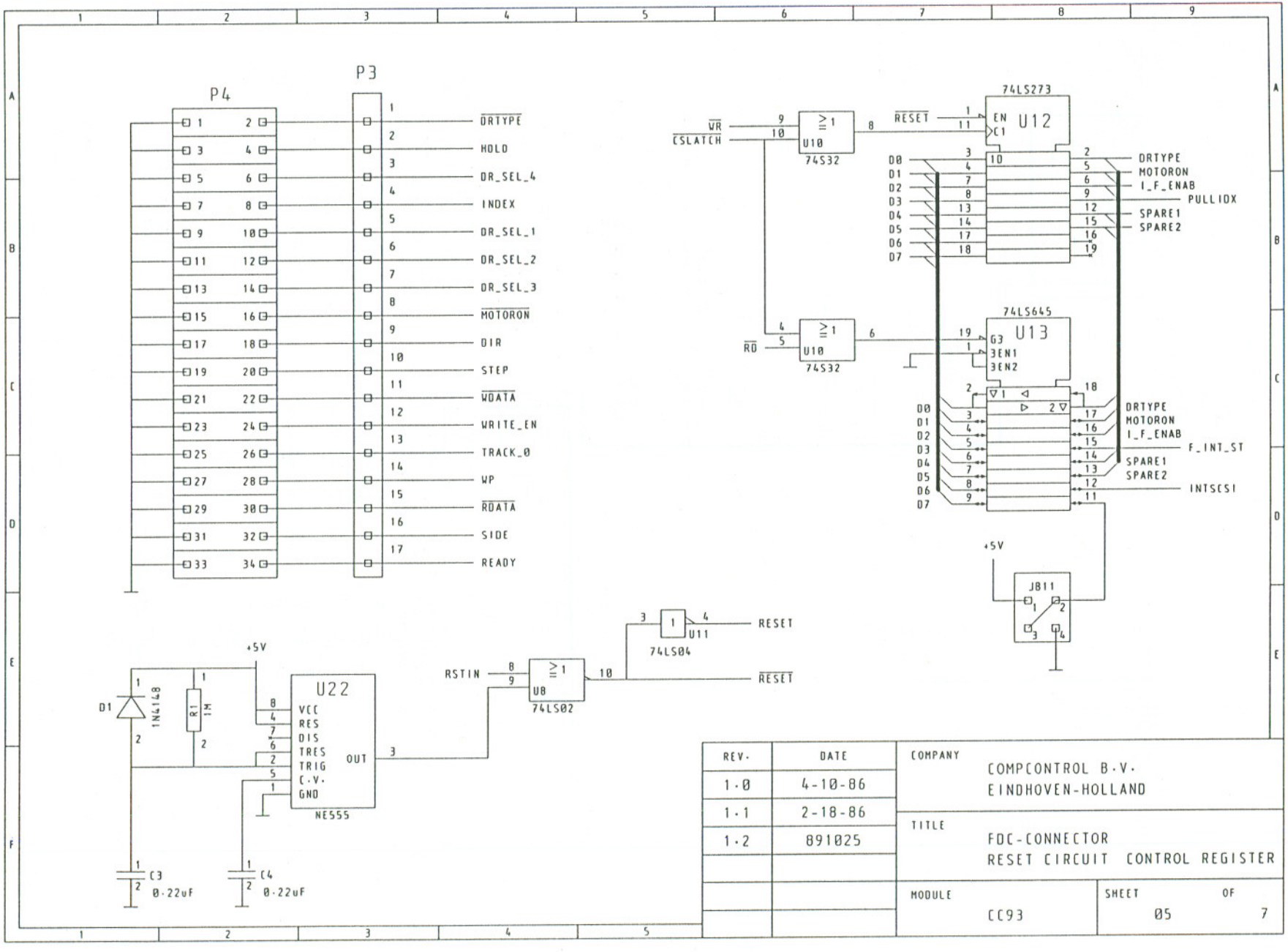
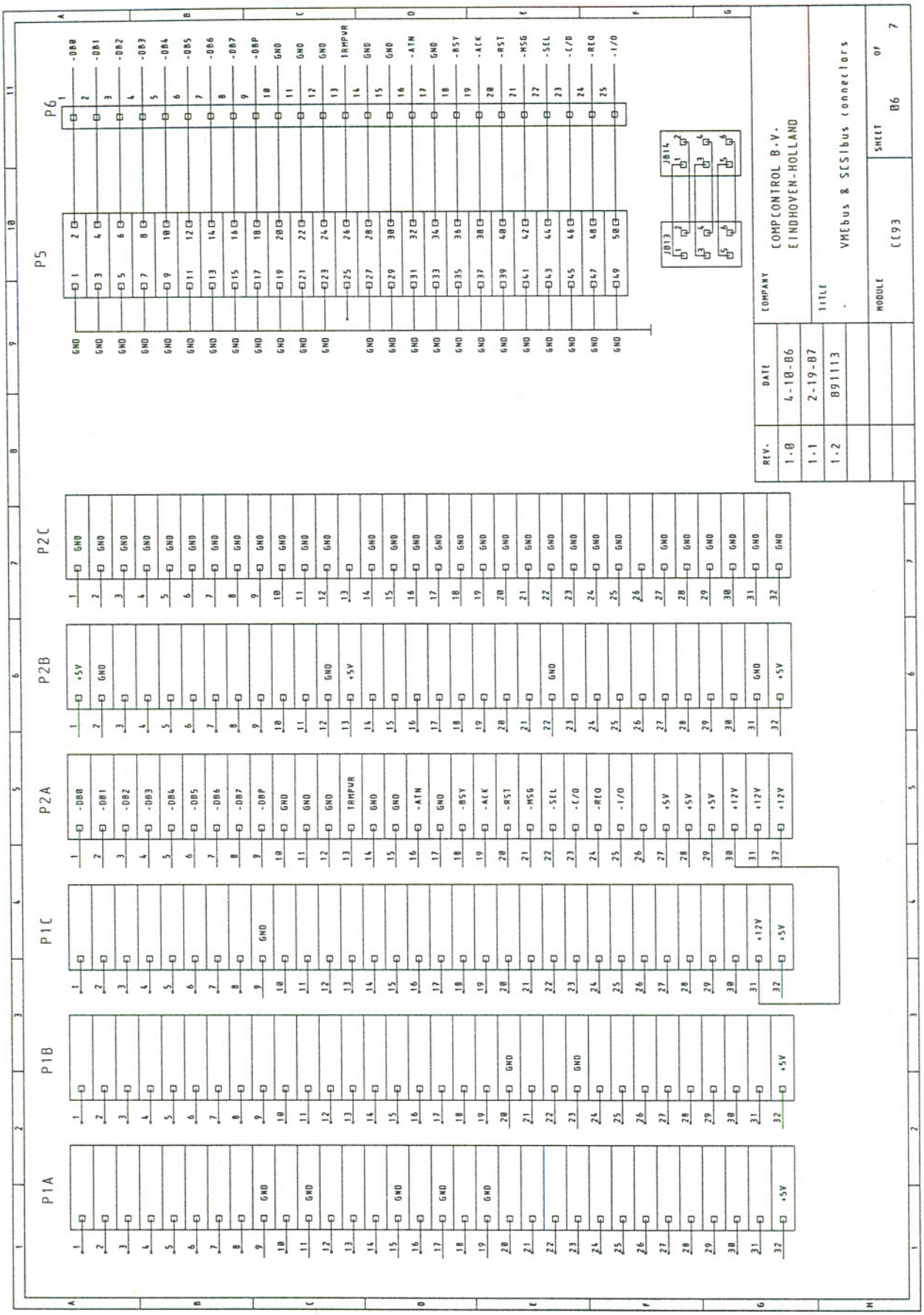
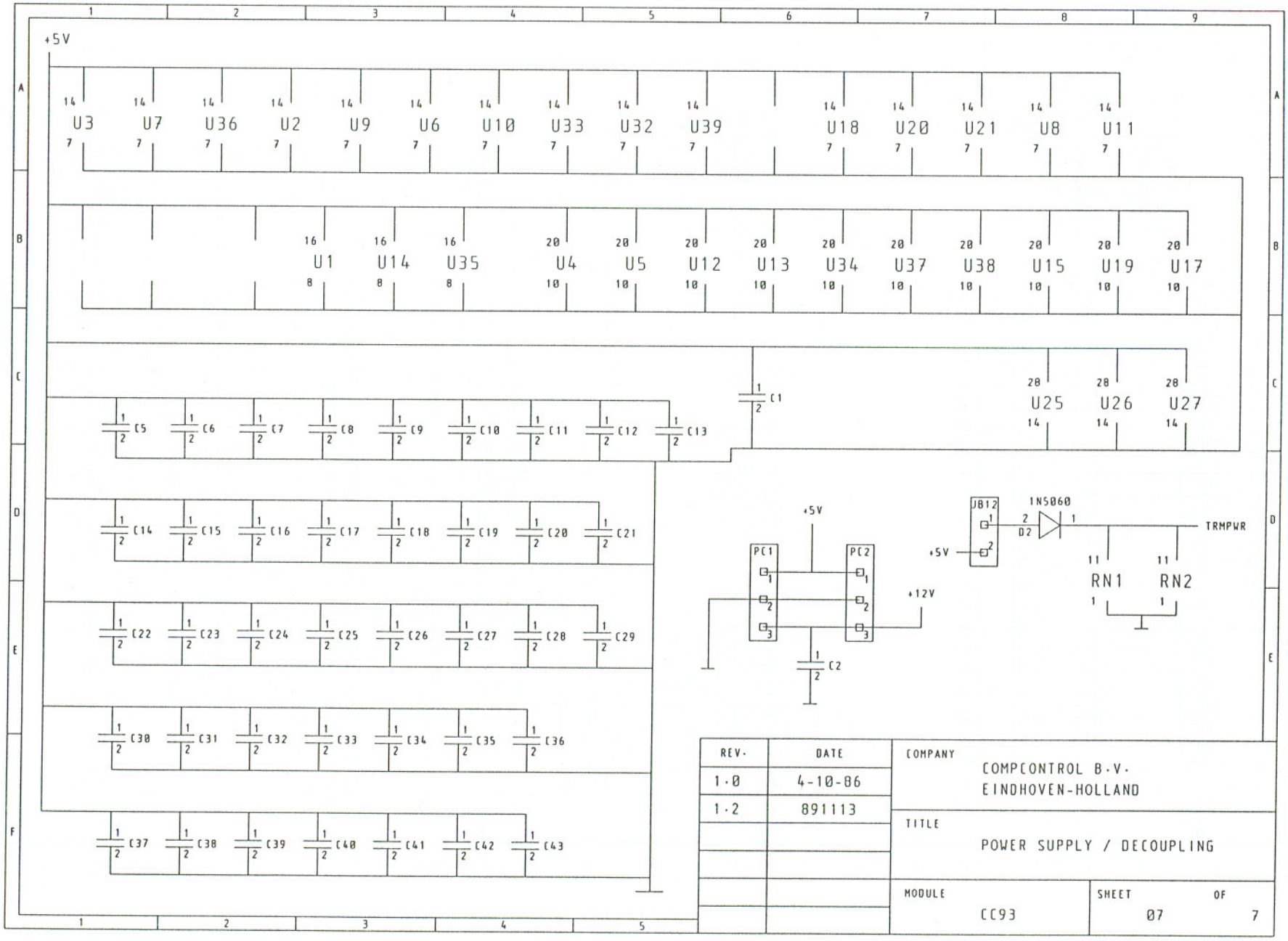
-DB3
-DB4
-DB5
-DB6
-DB7
U14
74LS148
ID0
ID1
ID2
RN4
U18
74S38
-DBP
-BSY
4K7
74F240
U17
-SEL
-RST
RSTIN
D0-D7
U16
NCR
5386
RESET
ATN
IGS
I/O
C/D
MSG
ACK
REQ
BSYOUT
SELOUT
RD
WR
DRQSCSI
TGS
DACK
TASCSI
74LS242
U20
-ACK
-ATN
U21
-I/O
-C/D
-MSG
-REQ
JB9
8MC
CSSCST
INTSCSI
U23
10MC
U7
7406
IRQ
REV.
DATE
1-0
4-10-86
1-1
11-21-86
1-2
891113
COMPANY
COMPCONTROL B.V.
EINDHOVEN-HOLLAND
TITLE
SCSI INTERFACE
MODULE
CC93
SHEET
04
OF
7

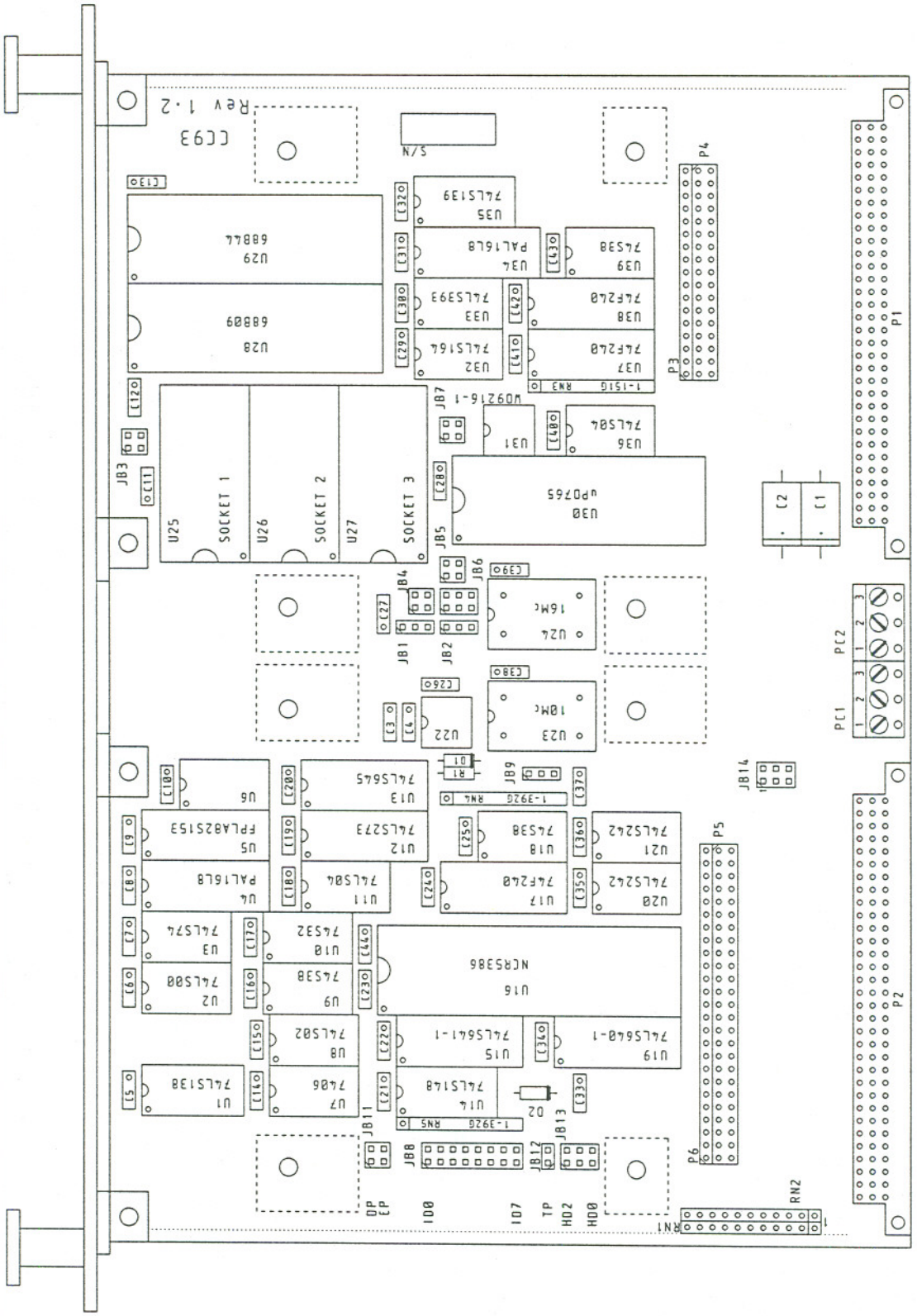

P4
P3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34
1 DRTYPE
2 HOLD
3 DR_SEL_4
4 INDEX
5 DR_SEL_1
6 DR_SEL_2
7 DR_SEL_3
8 MOTORON
9 DIR
10 STEP
11 WDATA
12 WRITE_EN
13 TRACK_0
14 WP
15 RDATA
16 SIDE
17 READY
VR
CSLATCH
U10
74S32
RESET
74LS273
U12
EN
C1
D0 D1 D2 D3 D4 D5 D6 D7
DRTYPE
MOTORON
I_F_ENAB
PULLIDX
SPARE1
SPARE2
RD
74LS645
U13
G3
3EN1
3EN2
DRTYPE
MOTORON
I_F_ENAB
F_INT_ST
SPARE1
SPARE2
INTSCS1
+5V
JB11
RSTIN
U8
74LS02
U11
74LS04
RESET
RESET
D1
1N4148
R1
1M
U22
VCC
RES
DIS
TRES
TRIG
C.V.
GND
OUT
NE555
C3
0.22uF
C4
0.22uF
REV.
DATE
1.0
4-10-86
1.1
2-18-86
1.2
891025
COMPANY
COMPCONTROL B.V.
EINDHOVEN-HOLLAND
TITLE
FDC-CONNECTOR
RESET CIRCUIT CONTROL REGISTER
MODULE
CC93
SHEET
05
OF
7


P1A
P1B
P1C
P2A
P2B
P2C
P5
P6
J813
J814
COMPANY
COMPCONTROL B.V.
EINDHOVEN-HOLLAND
TITLE
VMEbus & SCSIbus connectors
MODULE
CC93
SHEET
06
OF
7
REV.
DATE
1.0
4-10-86
1.1
2-19-87
1.2
891113


+5V
U3 U7 U36 U2 U9 U6 U10 U33 U32 U39 U18 U20 U21 U8 U11
U1 U14 U35 U4 U5 U12 U13 U34 U37 U38 U15 U19 U17
U25 U26 U27
C1 C2 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43
PC1 PC2
+12V
JB12
1N5060
D2
TRMPWR
RN1 RN2
REV. 1.0 1.2
DATE 4-10-86 891113
COMPANY COMPCONTROL B.V. EINDHOVEN-HOLLAND
TITLE POWER SUPPLY / DECOUPLING
MODULE CC93
SHEET 07 OF 7

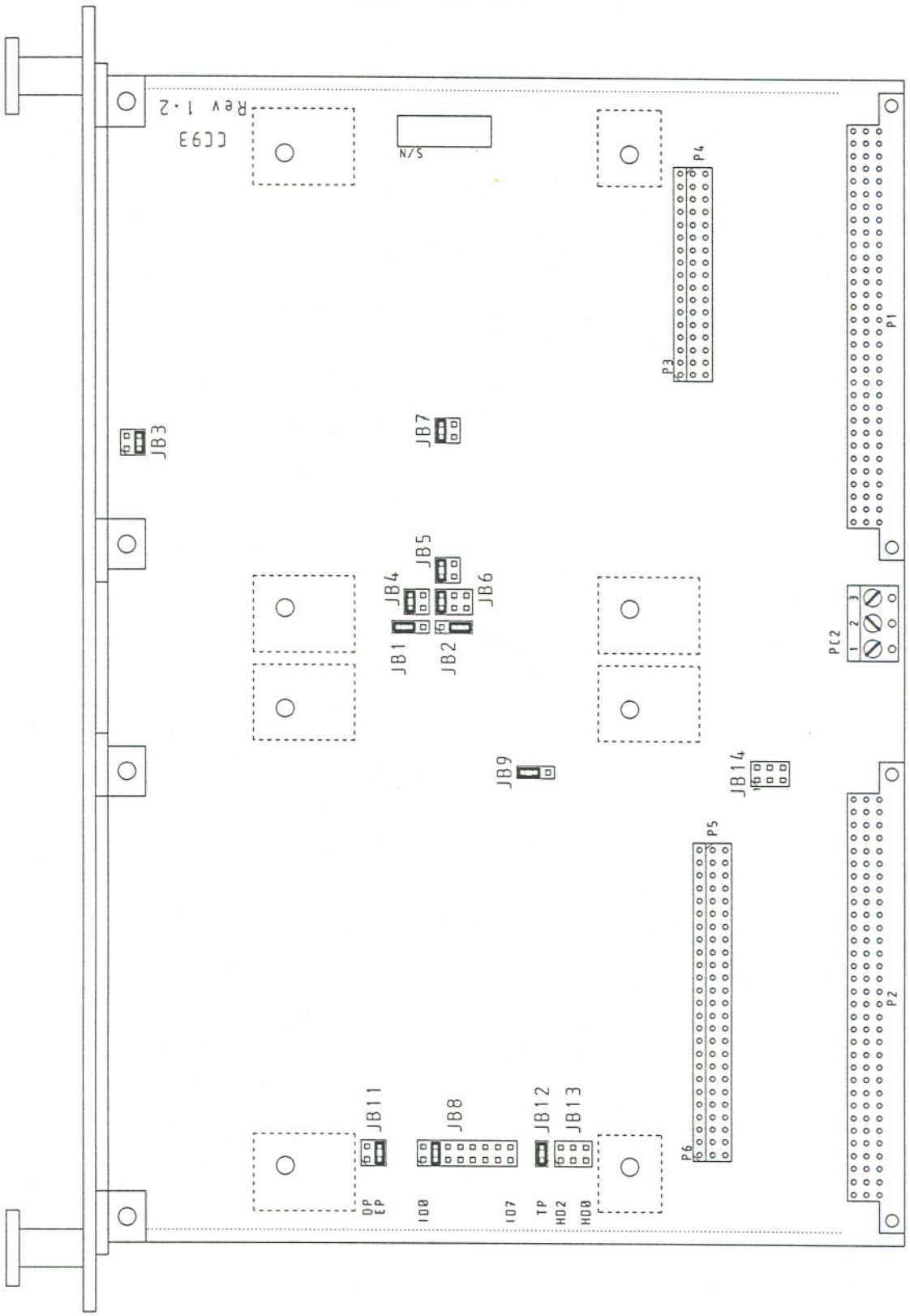
APPENDIX C

COMPONENT LAYOUT



APPENDIX C

JUMPER LOCATIONS



APPENDIX D

LIST OF COMPONENTS

Integrated Circuits (TTL)

U1	74LS138	DECODER
U2	74S00	NAND GATE
U3	74LS74	FLIP-FLOP
U6	74S00	NAND GATE
U7	7406	INVERTER O.C.
U8	74LS02	NOR GATE
U9	74S38	NAND GATE
U10	74S32	OR GATE
U11	74LS04	INVERTER
U12	74LS273	FLIP-FLOP
U13	74LS645	BUS TRANCEIVER
U14	74LS148	ENCODER
U15	74LS641-1	BUFFER
U17	74F240	BUFFER
U18	74S38	NAND GATE
U19	74LS640-1	BUFFER
U20,U21	74S242	BUS TRANCEIVER
U31	WD9216-01	DATA SEPARATOR
U32	74LS164	SHIFT REGISTER
U33	74LS393	COUNTER
U35	74LS139	DECODER
U36	74LS04	INVERTER
U37,U38	74F240	BUFFER
U39	74S38	NAND GATE

Integrated Circuits (PLD)

U4	16L8A-2	PAL
U5	82S153	FPLA
U34	16L8A-2	PAL

Integrated Circuits (Miscellaneous)

U16	NCR5386	SCSI CONTROLLER
U22	NE555	TIMER
U23	KX0-01-10	CLOCK OSCILLATOR
U24	KX0-01-16	CLOCK OSCILLATOR
U28	68B09	MICROPROCESSOR
U29	68B44	DMA CONTROLLER
U30	UPD765	FD CONTROLLER

Memory Devices

U25-U27	0-0640362-3	28 PIN SOCKET

Capacitors

C1,C2	100 uF	Capacitor, electrolytic
C3,C4	220NF/63V	Capacitor
C5-C43	0.1 uF	Bypass capacitor
C44	22NF	Capacitor

Resistors

R1	1 MOhm	Resistor

Resistor Networks

RN1,RN2	4611X-104-221/331	220/330 Ohm, 11-pin SIP
RN3	DALE 1-151G	150 Ohm, 10-pin SIP
RN4,RN5	MSP10A01-392G	3.9 KOhm, 10-pin SIP

Miscellaneous

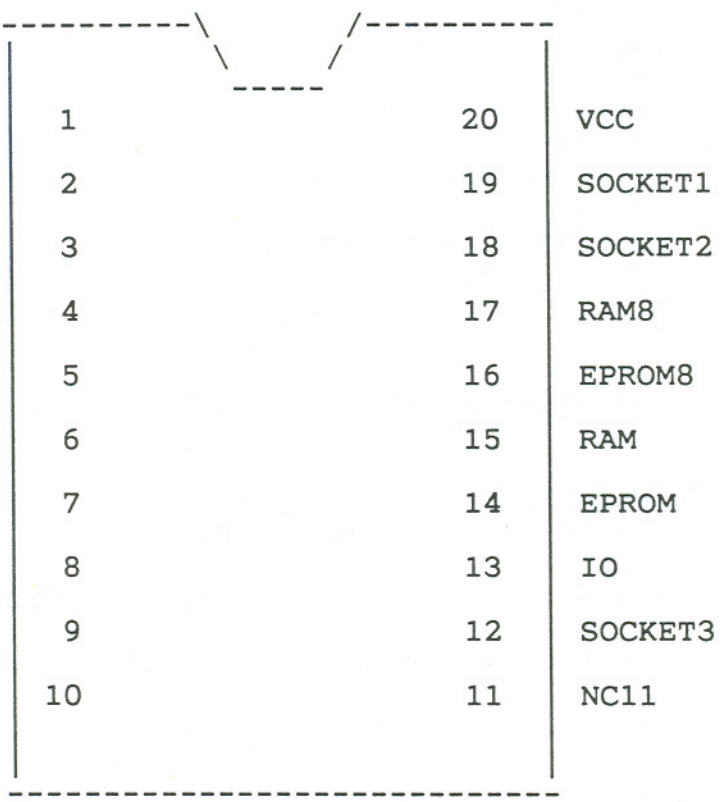
D1	1N4148	DIODE
D2	BYV10-30	DIODE
JB1,JB2	3-pin	Jumper block (1 x 3)
JB3-JB5	4-pin	Jumper block (2 x 2)
JB6	6-pin	Jumper block (2 x 3)
JB7	4-pin	Jumper block (2 x 2)
JB8	16-pin	Jumper block (hor) (2 x 8)
JB9	3-pin	Jumper block (1 x 3)
JB11	4-pin	Jumper block (hor) (2 x 2)
JB12	2-pin	Jumper block (hor) (2 x 1)
JB13	6-pin	Jumper block (hor) (2 x 3)
JB14	6-pin	Jumper block (hor) (2 x 3)
P1,P2	96-pin	IEC-603 male connector
P3,P4	34-pin	Jumper block (hor) (2 x 17)
P5,P6	50-pin	Jumper block (hor) (2 x 25)
PC1,PC2	WKS 17-06-A	T&B POWER CONNECTOR

APPENDIX E

MEMORY MAP

A description is given of the use of the F82S153 and the programming of this device.

F82S153



For the three signals /IO, /EPROM and /RAM addresslines A8-A15 and /VMA are used to decode the three parts of memory. Highest priority has the /IO signal. When /IO becomes active neither /RAM nor /EPROM may become active. All outputs are active low.

EPROM MAP: choose a lower boundary address for the EPROM map. Program /EPROM to be active on all addresses higher than and the same as this lower boundary.

RAM MAP: choose a upper boundary address for the RAM map. Program /RAM to be active on all addresses lower than this upper boundary.

IO MAP: use all eight addresslines A8-A15 to define an IO base address. A block of 256 bytes is now reserved for I/O; this block of memory is automatically locked out for RAM or EPROM.

FPLA specifications used for example memory map.

```
module PAL1;
flag '-r3','-V','-XH';
title  'MEMORY SELECTOR    COMPCONTROL B.V. EINDHOVEN';
"PAL DESIGN SPECIFICATIONS J.H. BRAND 2-4-1986
C93P1R0 device 'F82S153';
"declarations
   H,L = 1,0;
   X = .X.;

          A15,A14,A13,A12,A11,A10,A9,A8,VMA
      pin 1,  2,  3,  4,  5,  6,  7, 8, 9;
          EPROM8,RAM8
      pin 16,    17;
          GND,VCC
      pin 10, 20;
          IO,EPROM,RAM
      pin 13,14,   15;
          SOCKET3,SOCKET2,SOCKET1
      pin 12,     18,     19;
          NC11
      pin 11;

 address = [A15,A14,A13,A12, A11,A10,A9,A8, X,X,X,X, X,X,X,X];

equations
"EXAMPLE CONFIGURATION: ---8 kbyte ROM--- ---16 kbyte RAM--- ---
"       IO =  F000-F0FF  EPROM <=  E000    RAM <=  3FFF

!IO      = !VMA &       (address>=^hF000) & (address<=^hF0FF);

!EPROM   = !VMA & IO &  (address>=^hE000) & (address<=^hFFFF);

!RAM     = !VMA & IO &  (address>=^h0000) & (address<=^h3FFF);

"socket equations are not altered for other memory configurations!!
"-------------------------------------------------------------!!

SOCKET1 = !RAM   & !RAM8   & (address>=^h0000) & (address<=^h7FFF)
        # !RAM   &  RAM8   & (address>=^h0000) & (address<=^h1FFF);

SOCKET2 = !RAM   & !RAM8   & (address>=^h8000) & (address<=^hFFFF)
        # !RAM   &  RAM8   & (address>=^h2000) & (address<=^h3FFF)
        # !EPROM & !EPROM8 & (address>=^h0000) & (address<=^h7FFF)
        # !EPROM &  EPROM8 & (address>=^hC000) & (address<=^hDFFF);

SOCKET3 = !EPROM & !EPROM8 & (address>=^h8000) & (address<=^hFFFF)
        # !EPROM &  EPROM8 & (address>=^hE000) & (address<=^hFFFF);

end PAL1;
```