TECHNICAL MANUAL CC97 VMEbus
68000/68010 PROCESSOR MODULE

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Documentation history

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CC-97 MODULE

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CHAPTER 1

General Information

1.1 Introduction

This manual provides general information, preparation for use, installation instructions and theory of operation for the CC-97 VMEbus processor module. This manual also includes basic information needed by Software Engineers to design and implement software for it.

1.2 Features

VMEbus Compatible

- Optional system controller (CC-101)
- 4-level software selectable DTB requester (ROR/RWD)
- 7-level interrupt handler, software programmable
- 7-level interrupt requester, software programmable
- Selectable base address for dual ported RAM
- SYSFAIL generation logic

Microprocessor

- Standard MC68010, 10 MHz
- Optional MC68000, 10 or 16 MHz

Onboard Memory

- Static RAM 128 Kbyte
- Optional battery backed up static RAM 64 Kbyte
- Onboard EPROM 256 Kbyte
- Dual ported RAM 2 Mbyte

Parallel I/O

- SCSI interface with DMA capability

Serial I/O

- 1 serial channel (asynchronous) on front and P2 connector (RS-232C)
- 1 serial channel (asynchronous) on P2 connector
- 2 serial channels (multi protocol) on P2 connector with DMA capability

Timing Circuits

- Real-time clock with battery backup and alarm function
- Three 16-bit programmable timer/counters

Miscellaneous Functions

- 512 byte EEPROM (for setup code)
- Reset and Abort switches on front panel
- Leds for HALT, SYSFAIL, BBSY, and 3 user leds on front panel
- Mailbox with interrupt capability

1.3 General Description

The CC-97 is a high performance VMEbus compatible processor module, designed for 16-bit VMEbus systems. It can be used as a single board computer in 'small' VMEbus systems, however the architecture makes it also an ideal CPU module for multi processor applications, where dual ported RAM and versatile interrupt capabilities are essential.

The large amount of onboard EPROM space makes it possible to add firmware code so the module can be used as a stand alone microcomputer, however it can also function as an intelligent I/O module for the SCSI bus or serial communication channels.
The SCSI bus gives a wide range of peripherals that can be interfaced such as hard/flexible disk drives, tape drives, optical disk drives, and also other computers with a SCSI interface.
The serial channels support bit oriented protocols such as HDLC/ADCCP, SDLC, X.25 etc. as well as character oriented protocols such as BISYNC, DDCMP, X.21. It also supports asynchronous data transfers from 50 baud to 38.4K baud and synchronous transfers up to 4 Mbit/s.

1.4 System Controller

The system controller functions for the VMEbus are not located on this processor module. These functions are located on a seperate printed circuit board (CC-101), which will be mounted at the back of the slot 1 connector. CC-101 will replace the PCB with terminating networks, if any. The CC-101 module has onboard (passive or active) terminating networks, which can be disabled, and also performs the normal system controller functions such as:

- Clock generation for the System Clock and Serial Clock.
- A 4-level bus Arbiter with priority or round robin arbitration scheme, and an arbitration time out circuit
- Power on and manual reset logic
- Bus time out circuit
- Connection for external reset switch

CHAPTER 2

Specifications

2.1 Introduction

The CC-97 is a highly integrated and high performance VMEbus processor module, where random logic and state machines are designed using 20 programmable logic devices (PLD's). The onboard I/O functions are designed with the most advanced peripheral chips. The following section gives an overview of the main parts that are used.

2.2 Used Components

MPU, 68000 or 68010 microprocessor with 32-bit data, address and stack registers, 16 Mbyte direct addressing range, running at 10 or 16 MHz.

The 68155 is a high speed asynchronous interrupt handler used for all VMEbus interrupt lines and seven local interrupt sources. Control registers determine which interrupts are masked and also the type of interrupt acknowledge response.

The interrupt requester is designed with a PLD and can place an interrupt at one of the seven VMEbus interrupt lines under software control. During the interrupt acknowledge cycle a software programmable Status/ID byte is placed on the VMEbus and the interrupt line is deasserted.

The local memory consists of 4 JEDEC sockets for 27512 type EPROMs, and 4 JEDEC sockets for 55257 type RAMs. This configuration gives a total RAM space of 128 Kbyte and a total EPROM space of 256 Kbyte.

The dual ported memory has a total capacity of 2 Mbyte, using 1 Mbit TC511000Z devices. The MPU as well as the DMA controller can access this memory without wait states.

The 68450 is a four channel DMA controller where one channel is used for the SCSI interface, two channels for the serial interface and one channel is free to use for memory-to-memory transfers.

The 68562 DUSCC (Dual Universal Serial Communication Controller) supports synchronous/asynchronous data transfers and multiple protocols. Send/receive DMA transfers are supported for one

channel (full duplex) or two channels (half duplex).

The 68681 DUART (Dual Asynchronous Universal Receiver Transmitter) has programmable operating mode and data format for each channel. It can operate at baudrates from 50 to 38.4K baud.

Real-time clock ICM7170, has full calendar with automatic leap year correction, software selectable 12/24 hour format and on-chip battery backup switchover circuit. The two types of interrupts that can be generated are, periodic interrupts at 100Hz, 10Hz, 1Hz etc. and alarm interrupts at specified day and time.

The SCSI interface uses the WD33C93 protocol controller, which can be used as an initiator or target and supports arbitration, disconnect, reconnect, and parity. The single ended termination option is used, which allows a total cable length of 6 meters. The SCSI data transfers are handled by the onboard DMA controller.

The X2404 EEPROM gives 512 bytes of setup code and specifies the data retention to be greater than 10 years.

2.3 VMEbus Options

DATA TRANSFER OPTIONS

- DTB MASTER A24,A16;D16,D8
- DTB SLAVE A24 ;D16,D8

REQUESTER OPTIONS

- ANY ONE OF RWD or ROR (DYN)
- ANY ONE OF R(0),R(1),R(2),R(3) (DYN)

INTERRUPT HANDLER OPTIONS

- INTERRUPT HANDLER (DYN)
- ANY ONE OF IH(1-7) (DYN)

INTERRUPTER OPTIONS

- ANY ONE OF I(1),I(2),I(3),I(4),I(5),I(6),I(7) (DYN)
- 8-bit STATUS/ID (DYN)
- ROAK

POWER OPTIONS

- 3.4 A MAX (2.6 A typ) at +5 VDC
- 0.4 mA MAX (0.14 mA typ) at +12 VDC
- 0.6 mA MAX (0.34 mA typ) at -12 VDC

PHYSICAL CONFIGURATION OPTIONS

- NEXP

ENVIRONMENTAL REQUIREMENTS

- Operating temperature: 0 to 70 degrees C
- Max operating humidity: 90 %

CHAPTER 3

Theory of Operation

3.1 Introduction

This chapter gives an overview of the internal workings of the CC-97 module, this may be useful for repair or performance measurements. The block diagram of the module is given in Appendix A and the schematic diagrams are given in Appendix B. An explanation of the functional modules will be given in the next sections.

3.2 MPU/DMAC

The MPU and DMAC are shown in sheet 1 (Appendix B). The data buffers and address latches are used to connect both devices to the local address bus of 23 address lines and the local data bus of 16 data lines.

3.3 Local Memory

Sheet 2 (Appendix B) shows the local RAM/EPROM space, where 28-pin byte wide memory devices are used. For EPROM the 64K x 8 (27512) type devices should be used, which give a total space of 256 Kbyte. For RAM the 32K x 8 (55257) type devices should be used, which give a total RAM space of 128 Kbyte. The 8 JEDEC devices are accessed, using the memory select signals M0L, M0H, M1L, M1H, M2L, M2H, and M3L, M3H for the memory blocks 0 - 3 and the lower and higher data lines respectively.

3.4 Interrupt Functions

The interrupt handler functions (sheet 3) are performed by the 68155 in conjunction with PLD4. PLD 5 performs the interrupter function, including the interrupt acknowledge daisy chaining.

3.5 Control Registers

All control registers (sheet 4) use the peripheral data bus to transfer data. Note that the Board Control Register (BCR, U23/U24), the Bus Request Register (BRR, U20/U21), and the Interrupt Request Register (IRR, U22/U21) will be cleared by a local reset. The IRR will also be cleared during an interrupt

acknowledge cycle. The Interrupt Vector Register (IVR, U25) is a write only register and does not have a hardware reset.

3.6 Address Decoding

PLD 3 is used to decode the local address lines and U35 to buffer the address lines of the peripheral devices. The address decoding on the VMEbus is performed by U37, which may generate the VBS signal, that is used by PLD 8 to select the dual ported RAM. Sheet 5 (Appendix B) also contains the address and data buffer to the VMEbus and the shared bus. The shared bus is used when accessing the dual ported memory, and during an interrupt acknowledge cycle to transfer the interrupt vector.

3.7 Bus Control

PLD 6, PLD 10, and U38 (sheet 6) perform the DTB requester functions, where the BRLV0, BRLV1 lines determine the bus request level that is used. The LBR line is used to signal that the local master (MPU or DMAC) wants to access the VMEbus.
PLD 7 is a state machine that performs the arbitration of the shared bus. PLD 9 is used to generate the enable and direction signals for the VMEbus control lines.

3.8 Peripheral Control

Sheet 7 (Appendix B) is used to make all chip select signals for the onboard peripherals. The DTACK and BERR response signals are generated by PLD 13 and PLD 14 for those peripherals which do not generate them.

3.9 Memory Control

The dynamic memory control circuits are shown in sheet 8 (Appendix B), where PLD 15 contains the memory sequencer and PLD 17, PLD 18, and PLD 19 are used as address multiplexers with internal refresh counters. PLD 17, PLD 18, and PLD 19 also decode the mailbox addresses. The memory array is shown in sheet 9.
Sheet 8 also contains the clock generation circuits, for DMAC, serial ports, MPU and registered programmable logic devices.

3.10 Peripherals

Sheet 10 (Appendix B) shows all peripherals with their control lines. Also the front panel user leds are shown here.

CHAPTER 4

Installation Procedure

4.1 Introduction

This chapter provides the preparation and installation instructions for the CC-97 processor module.

4.2 Installation

The module can be used in VMEbus compatible systems and can be configured to suit many applications. Most options are selected by software. Options that depend on the installed hardware devices and need no change during operation of the module are selected by jumpers. The jumper block positioning and default jumper settings are illustrated in Appendix C. The pin definitions of the VMEbus P1, P2, and the I/O connector P3 will be found in Appendix G.

NOTE : BE SURE POWER IS TURNED OFF WHEN INSERTING THE CC-97 MODULE IN THE SYSTEM BACKPLANE.

4.3 Jumper Settings

All jumper settings, discussed in the following sections, are illustrated as seen from the component side with both VMEbus connectors downwards. Jumper blocks are drawn using a 'o' for each pin except pin 1 which is identified as '*'. The next table gives a summary of the default jumper settings and their function.

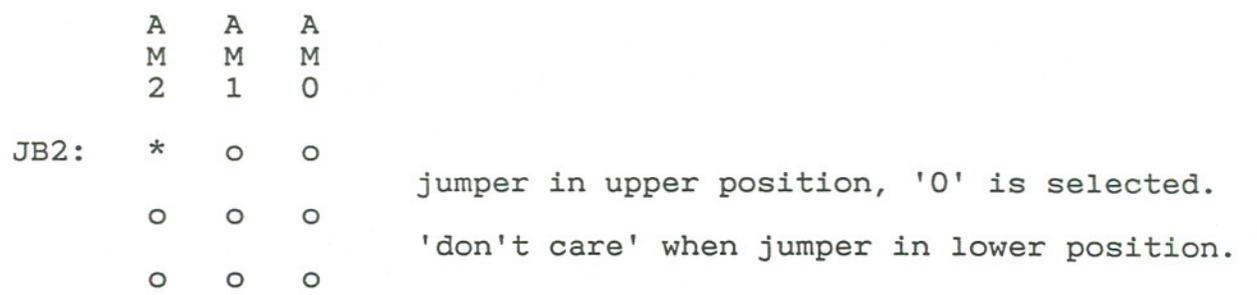
DESCRIPTION	JUMPER BLOCK	DEFAULT SETTING	STATUS	SECTION
VME RESET	JB1	1-2 CONNECTED	ENABLED	4.3.1
AM DECODING	JB2	4-7,2-5 CONNECTED	DATA ACCESS	4.3.2
MEMORY TIMING	JB3	NOT CONNECTED	SLOW ACCESS	4.3.3
SERIAL I/O	JB4	2-3 CONNECTED	FULL DUPLEX DMA	4.3.4
SERIAL I/O	JB5	2-3 CONNECTED	FULL DUPLEX DMA	4.3.4
MPU CLOCK	JB6	1-2 CONNECTED	10 MHz	4.3.5
SCSI RNPWR	JB7	1-2 CONNECTED	LOCAL +5V	4.3.6

4.3.1 VME Reset

Jumper JB1 is used to select if the VME reset line should be asserted during a local reset or not. In a single processor VMEbus system it will be usefull to reset the VMEbus whenever the onboard reset switch is pressed.

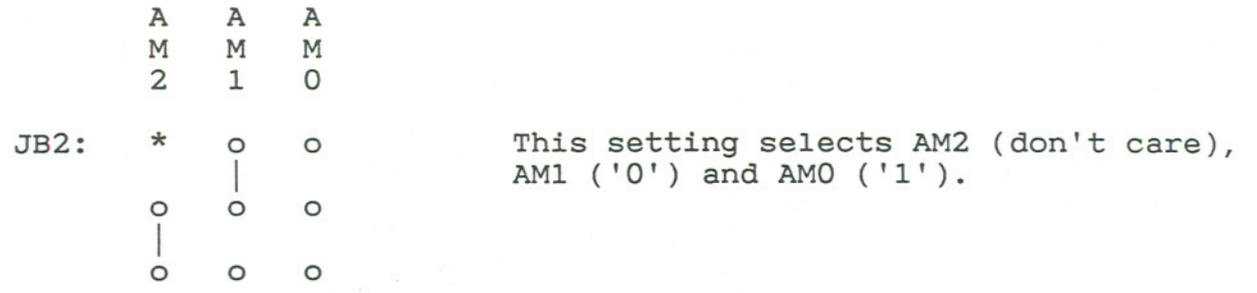
4.3.2 AM Decoding

Jumper block JB2 is used to select the AM code(s) to which the onboard dual port RAM should respond. All AM codes defined for standard addressed devices can be installed, except for VME block transfers, which are not supported. This means that the AM code lines AM3-AM5 should be high, where the AM code lines AM0-AM2 can be selected with JB2. These AM0-AM2 lines are selected to be low, don't care, or high.



When no jumper is installed, '1' is selected.

Example:



This setting selects standard supervisory as well as non-priviledged data access (AM codes $3D and $39).

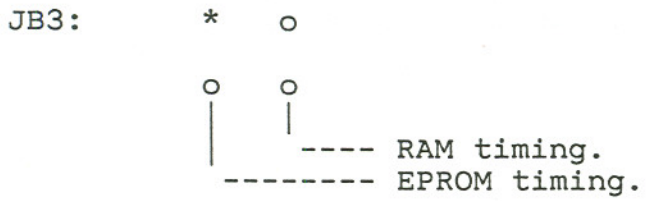
4.3.3 Memory Installation and Timing

The local memory is installed in 'stacked sockets', where each socket can hold two devices. Devices placed first in these sockets are mapped at the lower addresses. For EPROM devices, the 27512 (64K x 8) type is used and should be installed in the sockets U10 and U12. For RAM devices, the 55257 (32K x 8) type is used and should be installed in the sockets U11 and U13. U10 and U11 contain the upper byte (D8-D15) devices and U12, U13 the lower byte (D0-D7) devices. A full installation will have 4 EPROM devices, giving 256 Kbyte EPROM space and 4 RAM devices giving 128 Kbyte RAM space.

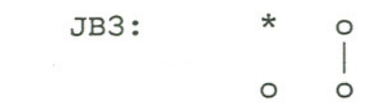
The timing for these static RAM and EPROM devices can be individually installed. JB3 is used to select this timing in terms of MPU clock cycles. When a jumper is installed, the local DTACK signal is immediately asserted after select, which gives a zero wait-cycle access. When no jumper is installed the local DTACK signal is asserted 4 clock cycles after select, which gives a three wait-cycle access.
Depending on the speed of the installed MPU, the following settings should be made. To select a setting, compare the 'chip enable access time' (Tce) for read, and the 'chip select to end of write time' (Tcw) for write to the figures in the table below. Both the maximum Tce from the data sheet and the minimum Tcw from the data sheet should be smaller than the numbers given below.
It will be clear that only the read timing will be significant for EPROM devices, and both read and write timing will be significant for RAM devices.

	10 MHz MPU memory timing	16 MHz MPU memory timing	Jumper JB3
Read (Tce)	175 ns	125 ns	Installed
Write (Tcw)	100 ns	60 ns	Installed
Read (Tce)	425 ns	300 ns	Not installed
Write (Tcw)	350 ns	210 ns	Not installed

Slow timing will be selected when no jumper is installed, fast timing will be selected when a jumper is installed.



Example:

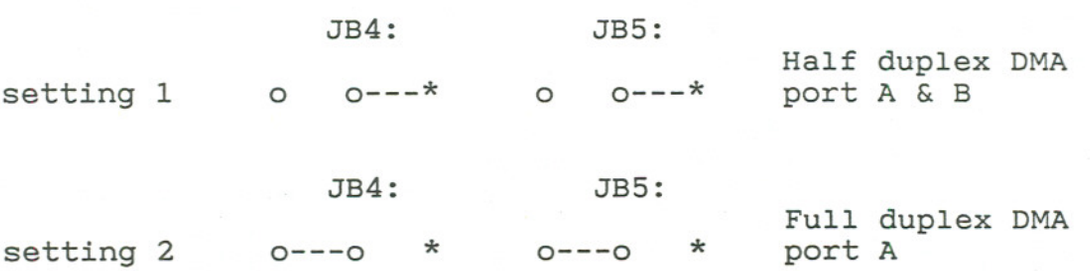


When a 10 MHz MPU is used, this setting assumes that the installed EPROMs have a Tce < 425 ns and installed RAMs a Tce < 175 ns and Tcw < 100 ns. For a 16 MHz MPU, these timing parameters are 300, 125, and 60 ns respectively.

4.3.4 Serial I/O DMA Transfers

Jumpers JB4 and JB5 are used to select which I/O ports (port A and/or B) of the DUSCC are supported by the DMA controller. The DMA controller has four DMA channels, where the channels 2 and 3 are used to support the DUSCC.

When full duplex DMA transfers are necessary, jumper setting 2 is used. With this setting received data of port A is transferred on DMA channel 2 and transmit data of port A transferred on DMA channel 3.
With jumper setting 1, half duplex DMA transfers are selected. With this setting the transmit AND receive data of port A is handled by DMA channel 2 and the transmit AND receive data of port B is handled by DMA channel 3.



Note that both jumpers (JB4 and JB5) always must be inserted in the same position.
The software implications of these jumper settings are discussed in chapter 5. The following table summarizes the pin usage of the request acknowledge functions of the DUSCC for each jumper setting, and also shows the DMA channel usage. The first table gives these functions for serial port A and the second table for serial port B.

DUSCC pin usage summary port A

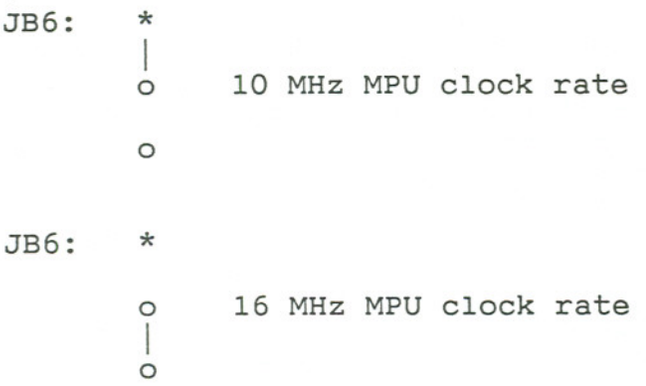
PORT A	Jumper setting 1		Jumper setting 2	
Function	Half duplex Single addr	Half duplex Dual addr	Full duplex Single addr	Full duplex Dual addr
RCVR REQ A	RTXDRQA_N DMA chan 2	RTXDRQA_N DMA chan 2	RTXDRQA_N DMA chan 2	RTXDRQA_N DMA chan 2
TRAN REQ A	same as RCVR REQ A	same as RCVR REQ A	TXDRQA_N DMA chan 3	TXDRQA_N DMA chan 3
RCVR ACK A	RTXDAKA_N DMA chan 2	Normal read RCVR FIFO DMA chan 2	RTXDAKA_N DMA chan 2	Normal read RCVR FIFO DMA chan 2
TRAN ACK A	same as RCVR ACK A	Normal write TRAN FIFO DMA chan 2	TXDAKA_N DMA chan 3	Normal write TRAN FIFO DMA chan 3

DUSCC pin usage summary port B

PORT B	Jumper setting 1		Jumper setting 2	
Function	Half duplex Single addr	Half duplex Dual addr	Full duplex Single addr	Full duplex Dual addr
RCVR REQ B	RTXDRQB_N DMA chan 3	RTXDRQB_N DMA chan 3		
TRAN REQ B	same as RCVR REQ B	same as RCVR REQ B		
RCVR ACK B	RTXDAKB_N DMA chan 3	Normal read RCVR FIFO DMA chan 3		
TRAN ACK B	same as RCVR ACK B	Normal write TRAN FIFO DMA chan 3		

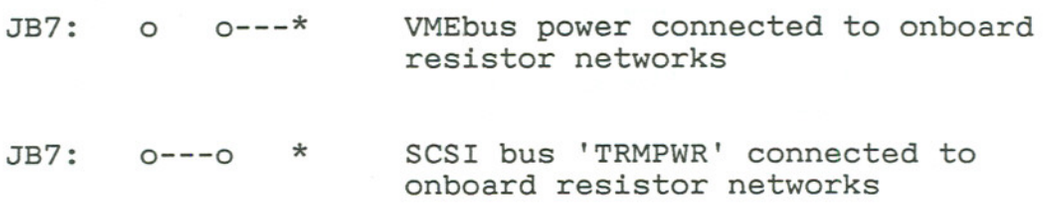
4.3.5 MPU Clock

Jumper JB6 is used to select the MPU clock rate. This jumper must be set according to the installed MPU type.



4.3.6 SCSI Bus Termination

The SCSI bus consists of a 50-pole flat-cable, which may be 'daisy chained' to a maximum of eight Initiator and/or Target devices. Both devices at the ends of the cable should have installed terminating networks and all other devices must NOT have these networks. The CC-97 module has the three relevant resistor networks, RN14, RN15, and RN16, installed in sockets, and these networks must be removed when the module is not at one of the ends of the daisy chain.
In some SCSI bus systems, the power of the terminating networks is supplied by a 'Terminating Power Supply' via pin 26 of the SCSI cable. This pin is referred to as 'TRMPWR. Jumper JB7 is used to select the power source for the onboard resistor networks.



4.4 I/O Connections

All I/O connections can be made through the P2 connector. One serial I/O channel is also available on a front panel connector P3, and is an RS-232C serial port, which can be used to connect a terminal. P3 is a flat-cable header with the proper pin definitions for an easy adaption to a 25-pin D-connector.
Appendix G shows the pin assignments of the I/O connectors P2 and

P3 and VMEbus connector P1.

When I/O connections are made, note that the serial I/O lines carry standard TTL signals, except for the serial I/O port that is also connected to P3. When using these TTL I/O lines the user is responsible to make the proper interface. This gives a wide range of interconnect possibilities, such as RS-232, RS-422, RS-485, optical interfaces etc.

CHAPTER 5

Programming Considerations

5.1 Introduction

This section contains all necessary information for system programmers to take full advantage of the features of the CC-97 module. The descriptions will include implementation dependent information that cannot be found in the respective data sheets. This chapter should be used in conjunction with the following references:

- Motorola MC68010 (MPU) data sheet
- Motorola MC68450 (DMAC) data sheet
- Signetics SCB68155 (Interrupt handler) data sheet
- Signetics SCN68681 (DUART) data sheet
- Signetics SCN68562 (DUSCC) data sheet
- Intersil ICM7170 (RTC) data sheet
- Western Digital WD33C93 (SBIC) data sheet
- XICOR X2404 (EEPROM) data sheet
- VMEbus specification, REV C.1

System programmers are expected to be fully conversant with all the material mentioned above and have the relevant experience, when they want to write their own system software.
In Appendix E, the MEMORY map of the CC-97 module is given, and Appendix F shows the I/O map.

5.2 Reset

When power is applied, the reset switch is pressed, or when the VMEbus SYSRESET signal is activated, all onboard devices will be reset. These include the MPU, DMA controller, Interrupt handler, board control register, bus request register, interrupt control register, startup circuit, DUART, DUSCC, and SBIC. The startup circuit will now force an EPROM select, so the MPU will fetch its initial program counter and supervisor stack pointer from the EPROM addresses 0-7. The following conditions exist now:

- The DMA controller, and other peripherals will terminate their operations, clear their internal storage elements, and fall into the idle state.
- The board control register wil be cleared and the VME SYSFAIL signal is driven, VME master access to the dual ported memory is inhibited, the Abort switch is disabled, the local Bus Time Out is disabled, Short AM code is disabled, and the SCSI Reset line is negated (NOT active).

- The bus request register is cleared and the bus release mode defaults to Always, which inhibits VMEbus access by the local master. The bus request level defaults to 0.
- The interrupt request register is cleared and will not generate an interrupt.

When an access (from the VMEbus) to the dual ported memory is in progress while a local reset is generated, this access will normally terminate.
Note that a MPU Reset instruction will not affect any device on the CC-97 module.

5.3 Status and Control

For the status and control signals four 8-bit registers are used. These ports are called BCR (Board Control Register), IVR (Interrupt Vector Register), BRR (Bus Request Register), and IRR (Interrupt Request Register). All registers will be seen an arbitrary number of times in the memory map, and are accessible at odd addresses as byte-wide memory mapped I/O devices. The addresses that should be used by system programmers are given in the next table.

Status/Control Register Summary

Address	R/W	Used Data Bits	Register Name
$060001	R/W	D0-D7	Board Control Register (BCR)
$060401	R/W	D0-D5	Bus Request Register (BRR)
$060801	R/W	D0-D3	Interrupt Request Register (IRR)
$060C01	W	D0-D7	Interrupt Vector Register (IVR)

5.3.1 Board Control Register

The board control register has the following bit definitions, which are discussed in the given sections.

Read Register	Write Register	Function	Section
bit 7 ABTFLG	bit 7 ---	Abort flag	5.14.1.1
6 SDA	6 ---	Serial data in	5.10.5
5 FAIL	5 FAIL	VME Sysfail	5.5
4 ABTRST	4 ABTRST	Abort reset	5.4
3 ELBTO	3 ELBTO	Enable local BTO	5.11
2 SRSTO	2 SRSTO	SCSI reset output	5.10.3
1 ESHRT	1 ESHRT	Enable short AM code	5.12
0 ENVA	0 ENVA	Enable VME access	5.7

Note: this is a R/W register where only bits 0-5 will read back the same as they were written. During a write to this register, bits 6 and 7 are discarded.

5.3.2 Interrupt Vector Register

The interrupt vector register is a write only register used to store the Status/ID byte that is used during an interrupt acknowledge cycle. This register should only be written if there is no pending interrupt request on the VMEbus. Section 5.15 will discuss the proper usage of this register.

5.3.3 Interrupt Request Register

Read Register	Write Register	Function	Section
bit 7 '1'	bit 7 ---	Not used	
6 '1'	6 ---	Not used	
5 '1'	5 ---	Not used	
4 '1'	4 ---	Not used	
3 ENIRQ	3 ENIRQ	Enable IRQ	5.15
2 ILV2	2 ILV2	Interrupt level	5.15
1 ILV1	1 ILV1	Interrupt level	5.15
0 ILV0	0 ILV0	Interrupt level	5.15

This register should only be written if there is no pending interrupt request on the VMEbus. An interrupt acknowledge cycle will clear this register and signals this condition. Section 5.15 will discuss the proper usage of this register.

5.3.4 Bus Request Register

The Bus request register has the following bit definitions.

Read Register	Write Register	Function	Section
bit 7 '1'	bit 7 ---	Not used	
6 '1'	6 ---	Not used	
5 '1'	5 SCL	Serial clock out	5.10.5
4 '1'	4 SDA	Serial data out	5.10.5
3 BRM1	3 BRM1	Bus release mode	5.13
2 BRM0	2 BRM0	Bus release mode	5.13
1 BRLV1	1 BRLV1	Bus request level	5.13
0 BRLV0	0 BRLV0	Bus request level	5.13

5.4 Abort Switch

The Abort switch, when pressed, may generate a non maskable interrupt. This non maskable interrupt (NMI) is also generated when a VMEbus ACFAIL signal is detected. The ABTRST bit in the BCR (bit 4 at $060001) controls the Abort switch function. Section 5.14.1.1 gives the interrupt handling information for the Abort and ACFAIL signals.

ABTRST	Abort switch function
0	disabled (default after Reset)
1	enabled

5.5 System Fail

The SYSFAIL signal on the VMEbus can be generated as well as detected by the CC-97 module. The SYSFAIL line on the VMEbus is monitored on the level 6 local interrupt input of the 68155 interrupt handler. This input can be polled or programmed to generate an interrupt, which is discussed in section 5.14.1.2.
The FAIL bit in the BCR (bit 5 at $060001) controls the SYSFAIL output on the CC-97 module.

FAIL	SYSFAIL line status
0	asserted (default after Reset)
1	negated

The front panel FAIL led will be ON when the FAIL bit is '0' and the VMEbus SYSFAIL line is asserted.

5.6 Local Memory

The local EPROM space runs from $000000 through $03FFFF, where the address locations $000000-$000007 will contain the initial Supervisor Stack Pointer and Program Counter. The local RAM space runs from $040000 through $05FFFF.
When a 68000 MPU is used, the vector table is located in the EPROM space. When a 68010 MPU is used, the vector table starts at the address in the Vector Base Register, and can be located anywhere in the memory map. After Reset the Vector Base Register is initialized at $000000.

5.7 Dual Ported Memory

The dual ported memory runs from $E000000 through $FFFFFF for the local MPU or DMAC and can be installed at any 2 Mbyte boundary for VMEbus masters. The dual ported RAM is designed in such a way, that the local MPU or DMAC may use the local bus (to access EPROM, Static RAM, or Peripherals) at the same time a VMEbus master accesses the dual ported memory. The ENVA bit in the BCR (bit 0 at $060001) is used to enable VMEbus masters to access the dual ported RAM.

ENVA	VMEbus access to Dual Ported RAM
0	inhibited (default after Reset)
1	allowed

When a VMEbus master accesses a dual ported RAM location while the ENVA bit is '0', the CC-97 module will not respond at all, which normally will result in a BERR response from the Bus Time Out module of the system controller.

5.8 Mailbox

The two lowest memory locations of the dual ported RAM are assigned to a so called mailbox. When a VMEbus master accesses this mailbox, a level 1 interrupt is generated to the local interrupt handler. Interrupt handling information is found in section 5.14.1.6.
It requires a PLD revision, when the mailbox must cover another address range or reside at a different address.

Note that the ENVA bit, discussed in the previous section also disables the Mailbox function.

5.9 DMA Controller

The DMA controller is located at the address locations $068000 through $0680FF and has four channels. The 4 channels are assigned to the SCSI controller and the DUSCC. The SCSI protocol controller is using DMA channel 0, where the DMA request and acknowledge signals are directly connected. The PCL0 line is connected to the interrupt output of the SCSI protocol controller. The DMAC can be used in single or dual addressing mode.
Channel 1 has no external request and acknowledge lines connected, and may be used in dual addressing mode for memory to memory transfers. The PCL1 line is connected to the SCSI reset line and may be programmed to generate an interrupt when a SCSI reset is detected. A SCSI reset will also directly reset the SBIC to conform to the SCSI specification.
Channel 2 is used for serial port A of the DUSCC and channel 3 for serial port A or serial port B. This depends on the use of full or half duplex DMA mode.

	Full duplex	Half duplex
DMA request chan 2	RTXDRQA_N	RTXDRQA_N
DMA acknowledge chan 2	RTXDAKA_N	RTXDAKA_N
DMA PCL chan 2	S2RDY	S2RDY
DMA request chan 3	TXDRQA_N	RTXDRQB_N
DMA acknowledge chan 3	TXDAKA_N	RTXDAKB_N
DMA PCL chan 3	S2RDY	S2RDY

The S2RDY (DUSCC READY) signal is in both modes connected to the PCL line of channel 2 and 3. These PCL lines must be programmed to function as a READY input for single address DMA modes. The DTC signal line of the DMAC is connected to the DTC line of the

DUSCC and the DONE signal line is also connected between the DMAC and DUSCC.

Further DMAC programming information can be found in section 4.3.4 (Serial I/O DMA Transfers) and section 5.14.1.4 (DMA Controller Interrupts).

5.10 Peripherals

All peripherals are 8-bit wide and are connected to the peripheral data bus (PD0-PD7). Peripherals are accessed at odd addresses, and use data lines D0-D7. When impliciet DMA addressing is used, data may also be transferred on the higher data lines (D8-D15). All peripherals and the DMA controller are located in the local I/O map at $06xxxx.

5.10.1 DUART Serial Interface

The 16 registers of the DUART are located at the addresses $063001 through $06301F. The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the MPU. The clock frequency for the DUART is 3.6864 MHz.

Port A is used as an RS-232C interface and has the signals TXD, RXD, RTS, and CTS. The DSR signal for port A is active when power is supplied to the CC-97 module. The port B receive and transmit lines, the input lines (IP1-IP5), and the output lines (OP1, OP3, OP5, OP7) are connected to the P2 connector. The other output lines are used to activate three user leds, where OP2 controls user led 0, OP4 controls user led 1, and OP6 controls user led 2. These Output Ports can be programmed to be high ('1') or low ('0'). When an output port is programmed to be low, the corresponding user led is ON. After Reset the OPx lines are all '1' and the user leds will be OFF.

5.10.2 DUSCC Serial Interface

The 68562 DUSCC has its internal registers mapped at the address locations $064001 through $06407F. The operation of the DUSCC is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the MPU.

Both channels of this device can be supported by the DMA controller, as described in section 5.9. The clock rate for the DUSCC is 14.7456 MHz.

5.10.3 SCSI Interface

The SCSI controller has a register file with 28 registers, which are indirect addressed at the memory locations $062001 and $062003. The interrupt line of the WD33C93 is connected to the PCL0 line of the DMA controller and can be polled or used to generate an interrupt (via the DMAC). The WD33C93 is reset when a local reset takes place and also when the reset line on the SCSI bus is activated. To make the processor aware of the reset condition on the SCSI bus, the SCSI reset line is connected to the PCL1 line of the DMA controller, and therefore may be programmed to generate an interrupt. The CC-97 module is also capable to activate the SCSI reset line, this is done by writing a '1' to the SRSTO bit of the BCR (bit 2 at $060001).

SRSTO	SCSI Reset Output
0	negated (default after Reset)
1	asserted

The WD33C93 has a 10 MHz clock rate.

5.10.4 Real Time Clock

The real-time clock is addressed at $061001 through $06103F, and has 18 byte-wide registers. The ICM7170 has its own 32.768 KHz X-tal and will hold time and date information using a lithium battery. Interrupts from this device are handled by the local interrupt handler on level 5, which is discussed in section 5.14.1.5.

5.10.5 EEPROM

The X2404 is a 512 byte EEPROM with serial data interface. All address lines are connected to ground. The clock input is programmed by writing to the SCL bit in the BRR (bit 5 at $060401). The data input is programmed by writing to the SDA bit in the BRR (bit 4 at $060401), and the data output can be read at the SDA bit of the BCR (bit 6 at $060001). A software protocol is used to read and write the contents of the EEPROM.

SCL	SCL Input of the EEPROM
0	0 (default after Reset)
1	1

SDA	SDA Input of the EEPROM
0	0 (default after Reset)
1	1

Note that the SDA and SCL bits in the BRR will always read back as '1'.

5.11 Bus Time Out

The Bus Time Out function is started when the local MPU or DMAC selects the local memory or onboard I/O, addressed at $000000 - $06FFFF. This circuit generates a local Bus Error when the accessed device does not respond within 8 us (10 MHz MPU) or 5 us (16 MHz MPU). An access to the VMEbus will normally start the bus time out circuit on the system controller module. The onboard dual ported memory does not have a local time out function.
The bus time out function is controlled by the ELBTO bit (Enable Local BTO) in the BCR (bit 3 at $060001).

ELBTO	Local Bus Time Out
0	disabled (default after Reset)
1	enabled

5.12 AM Code Generation

When the local MPU or DMAC accesses the VMEbus, their respective function code lines FC0-FC2 are used to generate the AM0-AM2 lines on the VMEbus. The AM3 and AM5 lines will never be driven and thus will be high when the CC-97 is the current VMEbus master. The AM4 line is high when the CC-97 accesses the VMEbus at the memory locations $080000 - $DFFFFF. The AM4 line can be high or low when the CC-97 accesses the memory locations at $07xxxx. When the AM4 line is low, it selects the VMEbus Short Address Space, where only address lines A1-A15 are significant. The ESHRT bit in the BCR (bit 1 at $060001) selects the state of the AM4 line during accesses at $07xxxx.

ESHRT	Short AM Code generation
0	disabled (default after Reset)
1	enabled

5.13 DTB Requester

The onboard DTB requester is used when the MPU or DMAC wants to access the VMEbus. The DTB requester can be programmed to use one of the four bus request lines. The bus release mode is also software selectable. The bus request register (BRR at $060401) is used to select the level with bits 0 and 1, and the bus release

mode with bits 2 and 3.

Bus request levels

BRLV1 (bit 1)	BRLV0 (bit0)	Bus Request level
0	0	0 (default after Reset)
0	1	1
1	0	2
1	1	3

Bus release modes

BRM1 (bit 3)	BRM0 (bit2)	Bus Release Mode
0	0	ALWAYS (default after Reset)
0	1	RWD
1	0	ROR
1	1	NEVER

When the bus release mode bits are cleared after reset or due to a write to the BRR, the DTB requester, when it has been assigned the VMEbus mastership, will release it as soon as possible and will not generate bus requests any more. This is an effective way to lockout the local MPU or DMAC of accessing the VMEbus. When a local master tries to access the VMEbus when the bus release mode is set to ALWAYS, a local bus error will be generated.

In RWD (Release When Done) mode, the DTB requester will release the VMEbus when the local master terminates the VMEbus access (i.e. after negation of address strobe).

In ROR (Release On Request) mode the DTB requester will only release the VMEbus when the local master terminates the transfer and another VMEbus master is asserting one of the bus request lines. When no other VMEbus module is requesting the VMEbus, the CC-97 DTB requester will not release the BBSY line and a next VMEbus access can be made without a VMEbus arbitration cycle.

In Release Never mode the DTB requester, when it has captured the VMEbus, will not release BBSY, until a write to the BRR changes the bus release mode. This is an effective way to lock the VMEbus for a longer period, and can be used to update global data without using semaphores.

5.14 Interrupt Handling

There are two types of interrupts, onboard and offboard interrupts. These interrupts are all processed by the 68155 interrupt handler. The 68155 has 8 registers which are accessed at $069001 - $06900F. The interrupts are prioritized in the following manner: local interrupt requests over VMEbus interrupt

requests with the non-maskable interrupt (NMI) considered the highest priority local interrupt (NMI over VMEbus IRQ7, then local IRQ6 - IRQ1 over VMEbus IRQ6 - IRQ1).

5.14.1 Onboard Interrupts

Interrupt level assignment

Level	Function	Vector supplied by	Section
7	ACFAIL, ABORT	68155	5.14.1.1
6	SYSFAIL	68155	5.14.1.2
5	RTC	68155	5.14.1.5
4	DUSCC	device (68562)	5.14.1.3
3	DUART	device (68681)	5.14.1.3
2	DMAC	device (68450)	5.14.1.4
1	MAILBOX	68155	5.14.1.6

The local interrupts are discussed in the given sections. The local interrupt acknowledge cycle should be programmed for 'device supplies the vector' mode for the local interrupts on level 2, 3, and 4. When this mode is used for the levels 1, 5, 6, and 7, the MPU will generate an autovectored interrupt acknowledge. These levels however may also be acknowledged with the mode where the 68155 supplies the vector (this method is recommended).

5.14.1.1 Abort and Acfail

The Abort switch signal and the VME ACFAIL signal are combined into a local NMI signal, which has the highest priority. It is a negative edge triggered interrupt, where the interrupt vector is supplied by the 68155. The interrupt routine must test the ABTFLG bit in the BCR (bit 7 at $060001) to determine the actual source of the NMI. When the ABTFLG is '1', the ACFAIL signal is the source of the NMI, otherwise the Abort switch has been pressed. The Abort switch signal is debounced and latched, therefore it is necessary that the interrupt routine clears this latch. This is done by writing a '0' in the ABTRST bit in the BCR (bit 4 at $060001), and then writing a '1' to this bit to enable the Abort switch again.

NOTE: The Reset condition for the Abort switch (ABTRST = '0') must be valid for at least 8 microseconds.

5.14.1.2 Sysfail

The SYSFAIL signal from the VMEbus is connected to the interrupt handler at the local (level 6) interrupt input. This interrupt input must be programmed to be active low and the 68155 should supply the vector during the acknowledge cycle. The SYSFAIL input can also be polled by the local MPU, wich is usefull at startup to determine if all VMEbus modules have released the SYSFAIL line.

5.14.1.3 Serial Ports

The two serial ports may generate their own interrupt at the levels 3 and 4 for the DUART and the DUSCC respectively. Both devices can generate a programmable vector during the interrupt acknowledge cycle, so the 68155 should be programmed to 'device supplies the vector' mode for these levels. The interrupt input lines must be programmed to be active low.

5.14.1.4 DMA Controller

The DMA controller uses the local interrupt line on level 2, and can generate a programmable vector during the interrupt acknowledge cycle. The 68155 must be programmed for 'device supplies the vector' mode, with the interrupt line to be active low.

5.14.1.5 Real Time Clock

The RTC can generate periodic interrupts as well as alarm interrupts, which are connected to the local interrupt level 5. The 68155 should be programmed to generate the vector during the interrupt acknowledge cycle. The interrupt line should be programmed to be active low.

5.14.1.6 Mailbox

The mailbox uses the local interrupt level 1. This interrupt should be programmed to be negative edge triggered and the 68155 must generate the vector during the interrupt acknowledge cycle.

5.14.2 Offboard Interrupts

The 68155 can handle the VMEbus interrupt lines IRQ1-IRQ7. The internal mask register is used to select which interrupt levels are handled by the CC-97 module.

5.15 Interrupter

The Interrupter is used to generate an interrupt at one of the seven VMEbus interrupt levels. When the VMEbus interrupt handler for this level acknowledges this interrupt, the interrupter will generate a Status/ID byte, deasserts the interrupt line (ROAK) and responds with DTACK.
When the CC-97 wants to place a VMEbus interrupt, it should first check if there is no pending interrupt by reading the Interrupt Control Register (ICR) and check bits 0 - 3 to be '0'. Then the IRQ level is written to the ICR with the ENIRQ bit '0', the interrupt Status/ID byte is written in the Interrupt Vector Register (IVR), and the IRQ level is written again in the ICR, but now with the ENIRQ bit '1'. This last write cycle will actually assert the selected interrupt line. During the interrupt acknowledge cycle for the generated interrupt, the Status/ID byte in the IVR is placed on the VMEbus and the ICR is cleared.

5.16 Self Diagnostic Method

When the CC-97 is powered on, it may run a diagnostic test before releasing the SYSFAIL line on the VMEbus. The stack frame is checked to see if a 68000 or 68010 is installed. The EEPROM can be read to retrieve setup information and the RTC to get the date and time. The board control and bus request registers are also setup now. The serial ports can be initialized, including the user leds. The peripheral chips, DMAC, and the memory should be tested. For testing the dual ported RAM, it is advised to access this memory through the local bus (at the addresses $E00000 - $FFFFFF) and also access the dual ported memory at its VMEbus address (installed with the hex switch). Both types of access can be made by the CC-97 itself, if the corresponding permission bits are properly set up.

For checking the interrupter and interrupt handler functions, the CC-97 may generate interrupts on the VMEbus that its local interrupt handler will acknowledge.

When all diagnostic code has been excecuted properly, the CC-97 should negate the SYSFAIL signal on the VMEbus and poll this line to check if all other modules also have released this line before proceeding normal program excecution.

5.17 MC68000 / MC68010 Differences

The next section discusses the most important differences between the 68000 and 68010. The 68010 has the next registers above those of the 68000:

- 1 32-bit vector base register
- 2 3-bit alternate function code registers

- 1 8-bit condition code register

The vector base register may be used to relocate the vector table.
The alternate function codes provide in a means for the supervisor to access user resources.
The condition code register has been added to secure supervisor resources from user access. The instruction 'MOVE SR,<ea>' is a priviledged instruction for the 68010. Users should use the new instruction 'MOVE CCR,<ea>' when they want to read the condition codes.
Another new instruction is RTD (ReTurn and Deallocate stack). Additional priviledged instructions are 'MOVE SR,<ea>' 'MOVEC' (MOVE Control register) and 'MOVES' (MOVE to alternate address Space).
In addition to the previous defined illegal opcodes for the 68000, the 68010 defines eight breakpoint illegal instructions with the bit patterns $4848-$484F.
The function code output lines (FC0, FC1, FC2) identify a CPU space cycle, when all are '1'. Interrupt acknowledge is identified as a CPU space cycle with also the address lines A16-A19 high. A breakpoint cycle is identified as a CPU space cycle with all the address lines A16-A19 low.

The 68010 uses another (not compatible) exception stack frame for the Bus error and Address error exceptions (group 0). Exception group 1 and 2 use a different but upward compatible stack frame. The stack frame for group 0 (except RESET) is given below for the 68000 and 68010.

	68000	STACK OFFSET	68010
SSP ->	access information	0	status register
	access address high	2	PC high
	access address low	4	PC low
	instruction register	6	format/vector offset
	status register	8	special status word
	PC high	A	fault address high
	PC low	C	fault address low
		E	unused, reserved
		10	data output buffer
		12	unused, reserved
		14	data input buffer
		16	unused, reserved
		18	instruction input buffer
		1A	internal info (16 words)

Execption vector 14 has been assigned for 'stack format error' for the 68010. This means that an illegal format code is retrieved from stack at offset 6.
The advantages of the 68010 are:

- Expanded supervisor capabilities.

- Relocation possibility of the vector table.
- Enhanced instruction execution timing due to high performance looping instructions.
- Alternate function code registers for both source and destination operands allow the supervisor to access user resources or emulate CPU space cycles.
- The 68010 supports virtual memory and has the capability to retrieve full processor information on bus error. This gives the possibility to rerun a failed access by software or hardware.